Analysis and simulation on measurement error of costas loop

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Abstract. In receiver design, how to choose the loop phase detector and loop filter carrier tracking loop is critical. Due to the Doppler frequency difference uncertainty exists, the carrier phase direct capture a greater degree of difficulty, and the frequency was able to capture most quickly eliminate the Doppler shift of the impact, and then the tracking phase is relatively easy to get many. Based on this idea, this paper, the performance of the PLL comprehensive analysis and simulation.

1 Introduction

In receiver design, how to choose the loop phase detector and loop filter carrier tracking loop is critical. Due to the Doppler frequency difference uncertainty exists, the carrier phase direct capture a greater degree of difficulty, and the frequency was able to capture most quickly eliminate the Doppler shift of the impact, and then the tracking phase is relatively easy to get many. Based on this idea, the paper on a comprehensive analysis of the performance of the phase locked loop.

2 A block diagram based on the phase locked loop

BPSK modulation signal input is provided:

$$R(k) = M(k)\cos(\omega_c k + \Delta\varphi) \tag{1}$$

Phase and quadrature branch output local NCOI were:

$$V_{Io}(k) = \cos(\omega_c k) \tag{2}$$
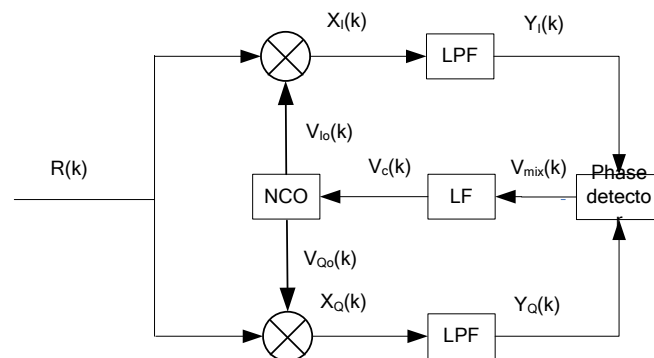
$$V_{Qo}(k) = \sin(\omega_c k) \tag{3}$$

Figure 1. costas loop block diagram

After a low-pass filter is,

$$Y_I(k) = \cos(\Delta\varphi) \tag{4}$$

$$Y_Q(k) = \sin(-\Delta\varphi) \tag{5}$$

When the phase difference is very small, its various phase detector within a certain range will show a linear shape characteristics. The phase error signal output by the loop filter:

$$V_c(k) \approx -2K_p\Delta\varphi \tag{6}$$

Wherein, K_p is the loop gain phase.

By equation (6) shows that the output frequency of the carrier NCO eventually be adjusted by the instantaneous phase difference.

3 Analysis and Simulation of Measurement Error

3.1 PLL thermal noise

Thermal noise has nothing to do with the order of the loop, thermal noise variance are:

$$\sigma_{tPLL} = \frac{360}{2\pi}\sqrt{\frac{B_L}{C/N_0}[1+\frac{1}{2TC/N_0}]}(°) \tag{7}$$

$$\sigma_{tPLL} = \frac{\lambda_L}{2\pi}\sqrt{\frac{B_L}{C/N_0}[1+\frac{1}{2TC/N_0}]}(m) \tag{8}$$

Wherein, B_L for the carrier loop noise bandwidth; C/N_0 for the carrier to noise power ratio; T is the integration time preflight; λ_L is the carrier wavelength.
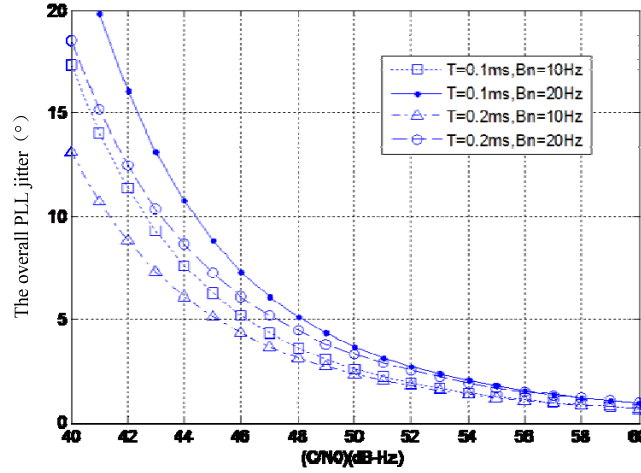

Figure 2. PLL thermal noise dither

Figure 2 is a preflight ramp times under 0.2ms and 0.1mm, for two different bandwidths for noise, PLL vibrate as a function of the thermal noise of the SNR.

3.2 Oscillator phase noise caused by vibration

Phase noise oscillator to vibrate the formula:

$$\sigma_V = \frac{360f_c}{2\pi}\sqrt{\int_{f_{min}}^{f_{max}} s_v^2(f_m)\frac{P(f_m)}{f_m^2}df_m}(°) \tag{9}$$

If the oscillator vibration sensitivity in the range of random vibration modulation frequency is not changed, then the formula (9) can be simplified as:

$$\sigma_V = \frac{360f_c}{2\pi}\sqrt{\int_{f_{min}}^{f_{max}}\frac{P(f_m)}{f_m^2}df_m}(°) \tag{10}$$

3.3 Allan variance oscillator phase noise

The general parameters of the instantaneous frequency offset segment is based on the Allan variance is defined as follows:

$$\sigma^2(\tau) = \frac{1}{2}E[(\frac{\varphi(z_{k+1}+\tau)-\varphi(z_{k+1})}{2\pi v_0\tau} - \frac{\varphi(z_k+\tau)-\varphi(z_k)}{2\pi v_0\tau})] \tag{11}$$

Where, τ is the sampling interval; E is the expected value operator; $\varphi(z)$ is the phase sampling sequence.

The phase noise of the Allan variance is defined as the formula:

$$\text{Two-step loop:} \quad \sigma_A = 144\frac{\sigma(\tau)f_c}{B_n}(°) \tag{12}$$

$$\text{Three-step loop:} \quad \sigma_A = 160\frac{\sigma(\tau)f_c}{B_n}(°) \tag{13}$$

Wherein, f_c is the operating frequency of the carrier (Hz); B_n is the equivalent noise

bandwidth (Hz); $\sigma(\tau)$ is Allan variance.

In the PLL, the design is narrow noise bandwidth to reduce the thermal noise in order to improve the tracking error threshold, however, as shown in equation (13), when the noise bandwidth is narrowed, the impact of the Allan variance dominant start position. For without the auxiliary carrier tracking loop is, Allan variance characteristics of the reference oscillator PLL reliably prevent poor work. Therefore, in the design of the carrier tracking loop, specifications oscillator Allan variance is very important.

3.4 Dynamic stress error

Dynamic stress error depends on the loop bandwidth and order. Having a minimum mean square error of two-step loop and three-step loop, its dynamic stress error is as follows:

$$\text{Two-step loop: } \sigma_{ePLL} = \frac{d^2R/dt^2}{\omega_n^2} = \frac{d^2R/dt^2}{(B_n/0.53)^2} = 0.2809\frac{d^2R/dt^2}{B_n^2}(°) \tag{14}$$

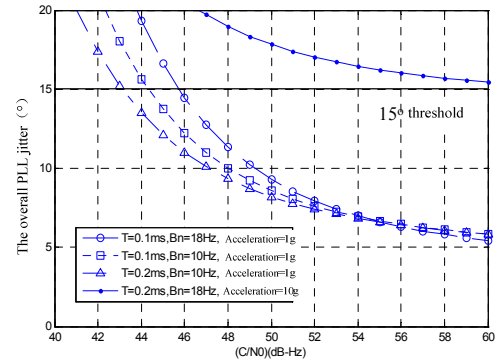$$\text{Three-step loop: } \sigma_{ePLL} = \frac{d^3R/dt^3}{\omega_n^3} = \frac{d^3R/dt^3}{(B_n/0.7845)^3} = 0.4828\frac{d^3R/dt^3}{B_n^3}(°) \tag{15}$$

Wherein, $\frac{d^2R}{d^2t}$ is the maximum dynamic radial acceleration($°/s^2$); $\frac{d^3R}{d^3t}$ is the maximum radial dynamic jerk($°/s^3$).

4 The total measurement error and PLL tracking loop threshold
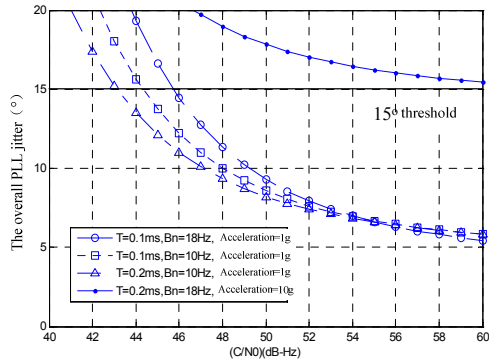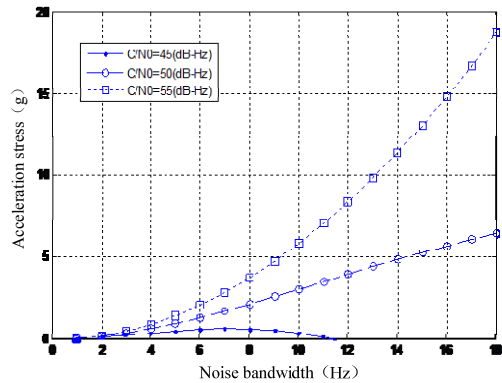

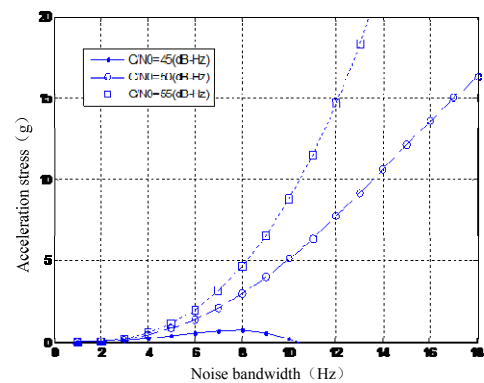(A). Second Order PLL jitter   (b). Third-order PLL jitter

Figure 3. Diagram simulation of PLL phase jitter and SNR relationship in different situations

Figure 3 (a) and 3 (b) describe the ring for the second order and third ring is used as the overall PLL phase jitter SNR function, including the impact of the type described. Wherein, $f_c = 2.2\text{GHz}$, vibration sensitivity $S_v = 1\times10^{-9}$, $P(f_m) = 0.005\text{g}^2/\text{Hz}$, $[f_{\min}, f_{\max}] = [10\text{Hz}, 2000\text{Hz}]$.

(a). Second Order PLL acceleration stress   (b). Third-order PLL jerk stress

Figure 4. Under different circumstances PLL noise bandwidth SNR and dynamic relationship between stress simulation map(T = 0.1ms, 15-degree threshold)

Figure 4 (a) and 4 (b) describe the second order and third-order PLL dynamic stress on the 150

limit. $f_c = 2.2 GHz$, vibration sensitivity $S_v = 1 \times 10^{-9}$, $P(f_m) = 0.005 \text{g}^2/\text{Hz}$, $[f_{\min}, f_{\max}] = [10\text{Hz}, 2000\text{Hz}]$.

The simulation, in the SNR = 55dB-Hz, second order phase-locked loop when the loop bandwidth equivalent to 4Hz, the dynamic stress of 20g signal phase tracking error is less than 3 degrees, the frequency tracking error is less than 1Hz.

5 Summary

This paper focuses on the performance of the PLL comprehensive analysis and simulation, including a brief description of PLL, oscillator phase noise and thermal noise and dynamic stress error detailed analysis and description of the last measurement error and the tracking ring threshold for a detailed policy analysis.

Reference

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