Study on Electrical Performance of FC and WB in IC Ceramic Package

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Abstract. As the signal frequency of integrated circuit keeps increasing, parasitic effects caused by the interconnect transmission structure used in IC ceramic package is becoming important factor which will influence the transmission performance of the signal path. In this paper, parasitic parameters (Resistance, Capacitance and Inductance) and scattering parameters of the differential pair are analyzed through three-dimensional electromagnetic software simulation based on the characterization of ceramic package structure. Then from the point of scattering parameters, the frequency domain whether wire bonding or flip chip is suitable is also analyzed. The result showed that the return loss of wire bonding interconnection would be great when the signal frequency is above 5GHz, and flip chip would improve the transmission performance of high-frequency signal remarkably when compared with wire bonding in the condition of same routing, and so flip chip is preferably in high-speed IC package.

Introduction

With the integrated circuit production process coming into the nanometer level, smaller size, faster processing speed and higher reliability become the development trend of IC industry. Higher frequency, increasing I/O number and smaller voltage margin made the high speed system design faced with great challenge, and put up higher requirements on high speed package. Problems could be neglected brought by package structure in the low speed system have become the restriction factor of the development of the high speed system. Parasitic effects caused by wire bond or flip chip interconnect used in ceramic package is becoming important factor which will influence the transmission performance of the signal path. So analysis of package structure's transmission performance has become indispensable important steps in the process of high speed system design and optimization.

At present, digital integrated circuit used in military and aerospace filed has reached 1500 pin level with computing speed reached 10 billion times per second, and the frequency of mixed signal circuits has reached above 3 GHz. Higher demand for design and process of ceramic package is proposed, ceramic package of high speed integrated circuits has become one of the bottlenecks of product development.

As the main interconnect modes between ceramic package and the chip, the parasitic effects of wire bond (WB) and flip chip (FC) will directly affect the signal integrity of high speed integrated circuit, and then affect the normal operation of the circuits. Thus, building propagation model and extracting the parasitic parameters is crucial for the design of high speed system.

In order to guarantee the normal operation of the chip, designers need selecting a suitable package method to make the work frequency of the chip contained in the package structure's suitable frequency range. Therefore, this paper firstly analyzed the parasitic effects theory of integrated circuit package, and then finished the modeling, parasitic parameters extraction and S parameter analysis of two different pairs of used 3D electromagnetic field simulation software. Those two differential pairs respectively used wire bond and flip chip interconnection, and in order to avoid different routing

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would influence on the results of the analysis, the routing are controlled nearly same. Finally, the adaptive frequency domain of wire bond and flip chip in ceramic package is concluded.

Parasitic Effects Theory

RLC parameters theory.

Bonding wire, bump, via, routing line and solder ball are the essential part of the signal transmission path in ceramic package. On the signal network, the parasitic resistance, capacitance and inductance of the interconnection structure will induce crosstalk and transmission delay of the signal, and they will induce IR drop, noise and PSRR of the circuits on power network.

Transmission lines used in the package design can be seen as strip line, which is shown in Fig.1.

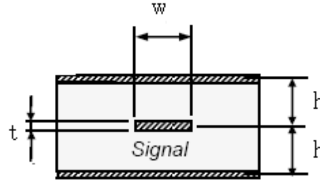

Fig.1 Strip line structure

The parasitic resistance, inductance, capacitance and the characteristic impedance can be respectively expressed as follows:

$$R = \frac{l\rho}{w\delta_s} \quad \Omega \tag{1}$$

$$C = 1017l\sqrt{\varepsilon_r} / Z_o \ pF \tag{2}$$

$$L = 1017l\sqrt{\varepsilon_r}Z_o \quad pH \tag{3}$$

$$Z_o = (60 / \sqrt{\varepsilon_r})ln\frac{8h}{0.67\pi w(0.8 + t / w)} \tag{4}$$

which ρ is the resistivity of routing metal， ε_r is the relative dielectric constant of the dielectric materials， δ_s is the skin depth and l is the length of the line.

Scattering parameters theory.

Scattering parameters is built on the relationship between incident wave and reflected wave. As the signal frequency is higher and higher, scattering parameters is increasingly used as transmission model in frequency domain to describe the properties of the transmission structure.

The amplitude of S11 is return loss caused by reflection, which is induced by the discontinuity. The smaller of its value, the smaller of the reflection, and the transmission performance will be better. Generally, S11 will less than 0.1 that is below -20dB. The amplitude of S21 is insertion loss, which is caused by the components insertion. The bigger of its value, the smaller of the transmission loss. The ideal value is 1 that is 0dB. Generally, while the value is above -3dB, that will guarantee the quality of signal transmission.

By the microwave transmission theory, the return loss and insertion loss of differential lines are shown as follows:

$$Return\ Loss = 20lg\left[\left|\frac{(Z^2 - Z_0^2)sh\gamma l}{2ZZ_0ch\gamma l + (Z^2 + Z_0^2)sh\gamma l}\right|\right] \tag{5}$$

$$Insertion\ Loss = 20lg\left[\left|\frac{2ZZ_0}{2ZZ_0ch\gamma l + (Z^2 + Z_0^2)sh\gamma l}\right|\right] \tag{6}$$

which Z is the impedance of the differential transmission lines, Z_0 is the target impedance of the differential lines, γ is the plural propagation constant and l is the length of the differential transmission lines.

Modeling and simulation

Structure design.

Structure design is the basis of package design; the first step of one product's package design is the confirmation of package form. In order to compare the effect on the electrical performance of high speed differential signal of wire bond and flip chip, this paper used wire bond and flip chip interconnect complete two alumina ceramic shell design, its structure diagrams are shown in Fig.2 and Fig.3 respectively.

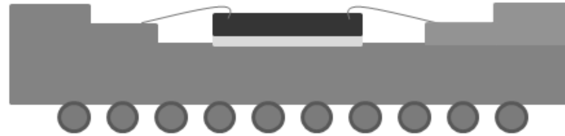

Fig.2 Wire bond interconnection structure

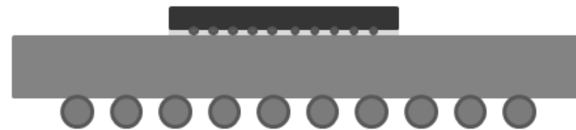

Fig.3 Flip chip interconnection structure

Modeling.

In order to compare those two different interconnection's influence on transmission performance of the differential path, the routing trace and the via in the signal path are controlled as consistent as possible.

Alumina ceramic substrate was adopted, which size is 12 mm*12 mm and its thickness is 1.25 mm. And Ball Grid Array (BGA) was adopted, the pitch of the solder ball is 0.8 mm and the diameter of the solder Ball is 0.5 mm. The package substrates is a 7 layers board design: the thickness of metal surface layer is 5.08 um and the thickness of routing metal layer is 10.16 um, which are all made in tungsten; the thickness of dielectric layer is 200 um; the first layer is the Top layer, the second floor is GND layer, the third layer is the Signal layer, the fourth layer for the power supply layer, the fifth floor is Land 1 layer, the sixth floor is Land2 layer, and the seventh layer is Bottom layer, and the cascade structure diagram is shown in Fig.4. This paper used Cadence APD software to complete the modeling of the whole differential transmission path: Case 1 adopted wire bonding, bond fingers are located on the third layer, and the model diagram is shown in Fig.5; Case 2 adopted flip chip, and the model diagram is shown in Fig.6. And the specific process parameters of bonding wires, bumps and BGA solder ball are shown in Tab.1.

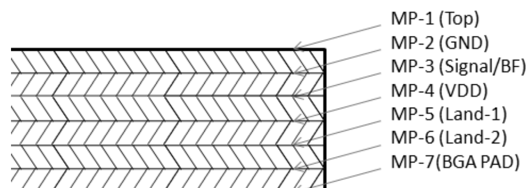

Fig.4 Diagram of the cascade structure

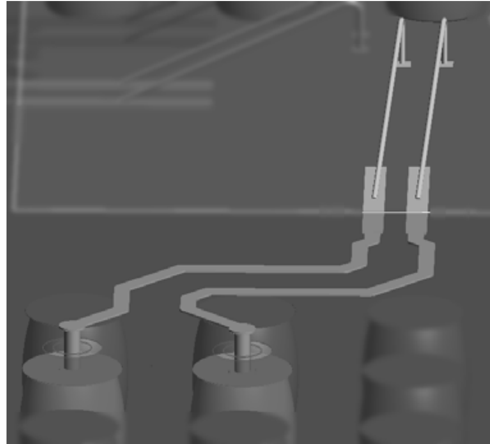

Fig.5 Model of gold wire bonding interconnect

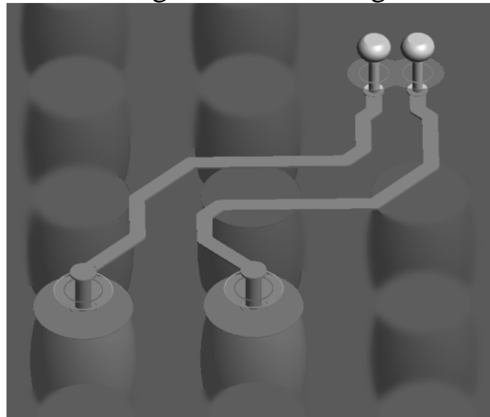

Fig.6 Model of flip chip interconnect

Tab.1 Parameters of package process

	Wire	Bump	Ball
Case 1	25um gold wire	/	0.5mm 90Pb10Sn
Case 2	/	110um 63Pb37Sn	0.5mm 90Pb10Sn

RLC extraction. Three-dimensional electromagnetic software was used to extract the parasitic parameters of the differential transmission path. Through solving Maxwell's equations in frequency domain, more accurate extraction of the parasitic parameters is reached. This paper completed the parasitic parameters extraction of the differential transmission path in the frequency of 100 MHz, the length of the routing trace, the parasitic resistance and the parasitic capacitance, the parasitic inductance, mutual capacitance and mutual inductance are shown in Tab.2

Tab.2 Parasitic parameters extraction

		L (um)	R (ohm)	C (pF)	C_{mutual} (pF)	L (nH)	L_{mutual} (nH)
Case 1	CLK_N	2315	0.649	1.240	0.641	5.456	6.600
	CLK_P	2305	0.656	1.235	0.641	5.292	6.600
Case 2	CLK_N	2312	0.519	1.110	0.556	3.599	3.769
	CLK_P	2300	0.512	1.096	0.556	3.421	3.769

Scattering parameters analysis. This papers also conducted extraction of scattering parameter, and the sweep frequency is set to 100MHz to 20GHz, and the insertion loss and the return loss were obtained.

The return losses of those two models are shown in Fig.7. Compared with flip chip interconnection, the reflection of wire bonding interconnection is significantly larger due to impedance mismatch, and the return loss will reach above -10dB when the frequency is above 5 GHz. And the reflection can be reduced by shorten the length of the bonding wires. And while the frequency is below 18.4 GHz, the return loss of the transmission path can be controlled below -10dB which can guarantee effective transmission of high speed signal.

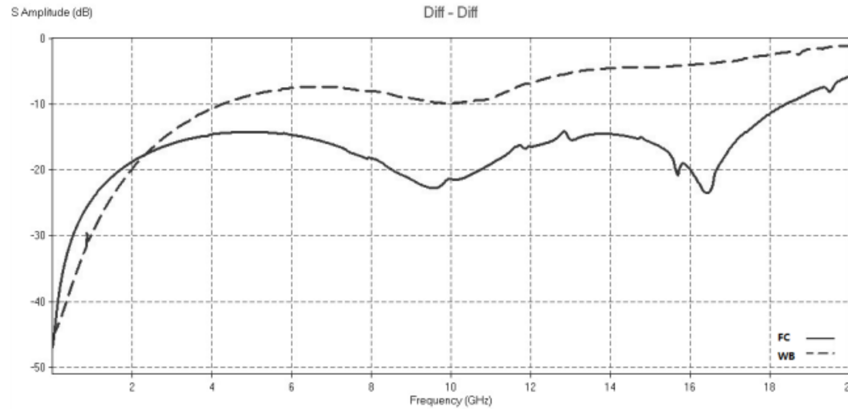

Fig.7 Comparison of return loss between two interconnection structures

The insertion losses of those two models are shown in Figure 8. Obviously, the insertion loss of flip chip interconnection is superior to wire bonding interconnection. Throughout the 100MHz to 20 GHz sweep frequency range, the insertion loss of flip chip interconnection can be effectively controlled above -3dB, which can guarantee the transmission of high speed signal. And the insertion loss of wire bonding interconnection will increase obviously when the frequency is above 15 GHz that is hard to meet the transmission of high speed signal.

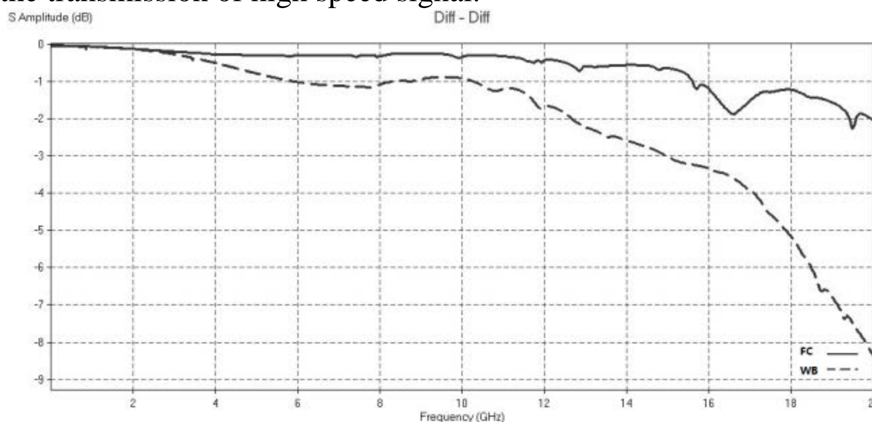

Fig.8 Comparison of insertion loss between two interconnection structures

Conclusions

This paper finished parasitic RLC parameters and S parameters extraction of two differential transmission path used wire bond and flip chip interconnect respectively on the basis of the alumina ceramic package, and flip chip interconnect can effectively reduce the parasitic effects. When the frequency is above 5GHz, the reflection of wire bond interconnect would be huge that is difficult to meet the transmission demand of high speed signal. All in all, flip chip interconnect has better electrical performance, which is more suitable for high speed integrated circuit ceramic package.

References

[1] G. G. Harman, "Wire bonding in microelectronics," McGraw-Hill, New York, NY, p. 46, 2010

[2] Y. K. Ho and Y. W. Chang, "Multiple chip planning for chip-interposer co-design," in Design Automation Conference (DAC), 2013 50th ACM /EDAC / IEEE, 2013, pp. 1 - 6.

[3] Y. Shuai, "Investigations on Microwave Characteristics of gold wire bonding and Via Interconnects Based on LTCC Technology," Xidian University 2012

[4] EVANS J, AMARATUNGA G. The behavior of very high current density power MOSFETs [J]. IEEE Trans Elec DEV, 1997, 44(7): 1148-1153.

[5] YOUNG B. Digital signal integrity：modeling and simulation with interconnects and package [M]. New Jersey：Prentice Hall，2001

[6] J.-W. Fang, C.-H. Hsu, and Y.-W. Chang, “An integer linear programming based routing algorithm for flip-chip design,” in Proc. Assoc. Comput. Machinery/IEEE Design Autom. Conf., Jun. 2007, pp. 606–611.