

# FPGA implementation of Reed-Solomon Codes Based on Visible Light Wireless Communication System

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**Abstract.** The research of visible light communications(VLC) has become a focus of wireless communications in recent years. In this paper, the channel coding technique for VLC systems were studied. According to the characteristics of VLC channel, RS codes were designed to correct the burst and random errors. The pipeline architecture was designed in the proposed system, and the RS decoder was divided into 4 modules, the syndrome calculation module, the key equation calculation module, the *Chein Search* module and the *Forney* algorithm module. In the Chein search module, the RiBM algorithm was used for reduction of complexity. All FPGA implementations of the 4 modules were provided in detail, and simulation results were shown on the Quartus II 9.0 platform. The simulation results show that, no more than 8 random and burst errors can be completely correct by one single proposed RS (204,188) codeword.

## Introduction

Visible light communication can transmit wireless information by using fast light pulse, such as coded '1' when the LED is on, otherwise coded '0'. VLC technology can be instead of conventional wireless communications in some places with forbidden of the electromagnetic interferences, such as airport, hospital etc. In a practical communication system, channel coding technology can provide a guaranteed coding gain, which can save the transmission power and increase the distance of communications.

Recently, in VLC channel analysis, system designing, modulation and signal detection have attracted much attention. As known, the burst errors occurred frequently in VLC system because of many indoor factors, like occlusion, fading and noise. In this paper, first we chose a RS code from Digital Video Broadcasting (DVB) standard for our VLC scheme in order to improve the quality of communications. Then the implementations of the RS encoder and decoder were proposed in detail, and some simulation results were presented to prove the effectiveness. At last, the experiments showed that the RS-based VLC system worked well on the FPGA Cyclone IV EP4CE15F17C8N.

## Visible Light Communication System

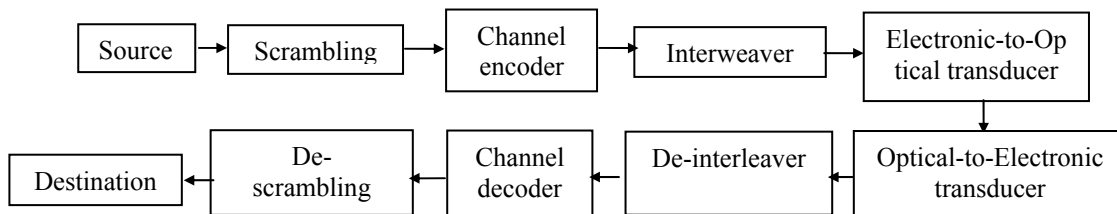


Fig. 1 VLC system process diagram

The diagram of VLC system is shown in Fig. 1. The optical transmitter consists of source, scrambling, channel encoder, interleaver and electronic-to-optical transducer. The information bits should be

processed before they transmitted. For example, the scrambling module eliminates continuous '0' or '1' in source information, the channel encoder module reduces BER during transmission, the interleaver module avoids the burst errors occurred. The electronic-to-optical transducer transfers electronic signal into optical signal. Correspondingly, the optical receiver is made up of optical-to-electronic transducer, de-interleaver, channel decoder, de-scrambling and destination. Receiver restores the processed information in correctly.

### Brief Introduction of RS Codes

**RS Encode.** Reed-Solomon (RS) code is a class of linear block codes, see [1]. So RS codes can be explained as non-binary BCH codes. The values of code coefficient are taken from  $GF(2^m)$ , refer to [2]. Let  $\alpha$  be the primitive element of  $GF(2^m)$ . For a  $t$ -error correcting RS codes, the roots of generator polynomial  $g(x)$  are  $\alpha, \alpha^2, \dots, \alpha^{2t}$ , and

$$g(x) = (x-\alpha)(x-\alpha^2)\cdots(x-\alpha^{2t}) = g_0 + g_1 \cdot x + \cdots + g_{2t-1} \cdot x^{2t-1} + x^{2t}. \quad (1)$$

Where  $g_0, g_1, \dots, g_{2t-1}$  are the coefficient of generator polynomial.

If un-coded information polynomial is

$$m(x) = m_0 + m_1 \cdot x + \cdots + m_{k-1} \cdot x^{k-1}. \quad (2)$$

Check polynomial

$$r(x) = r_0 + r_1 \cdot x + \cdots + r_{n-k-1} \cdot x^{n-k-1}. \quad (3)$$

Where  $k$  is the number of information bits,  $n$  is code length.

Thus we can get code polynomial

$$c(x) = x^{2t}m(x) \bmod g(x). \quad (4)$$

The design of RS codes encoder is shown in Fig. 2.

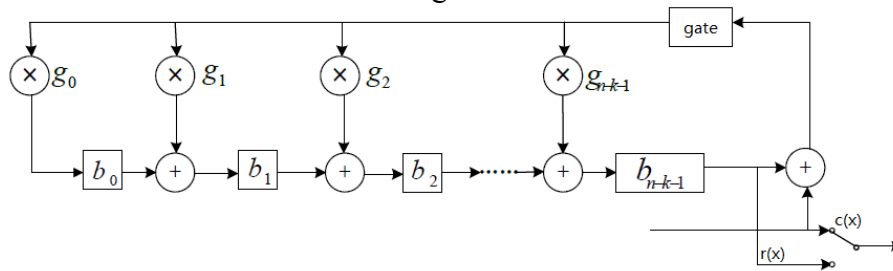


Fig. 2 RS codes encoder schematic diagram

**RS Decode.** When decoder receive the signal  $R(x)$  from channel, it need to detect and correct errors in  $R(x)$ . The processing of decode as follows: First, receiving  $R(x)$  and get syndrome  $S_i$  by equation (5). Secondly, according to  $S_i$ , using BM algorithm given in [3] to get error position polynomial  $\Lambda(x)$  and error value polynomial  $\Omega(x)$ . Thirdly, using Chien Search, given in [4], to detect the positions of errors. Forth, calculating errors' value by Forney equation in [5]. Finally, synthesizing errors' position and value. Then we can get the corrected result  $c'(x)$ . If  $c'(x) = c(x)$ , decode succeed, or fail. The schematic design of decoder is shown in Fig. 3.

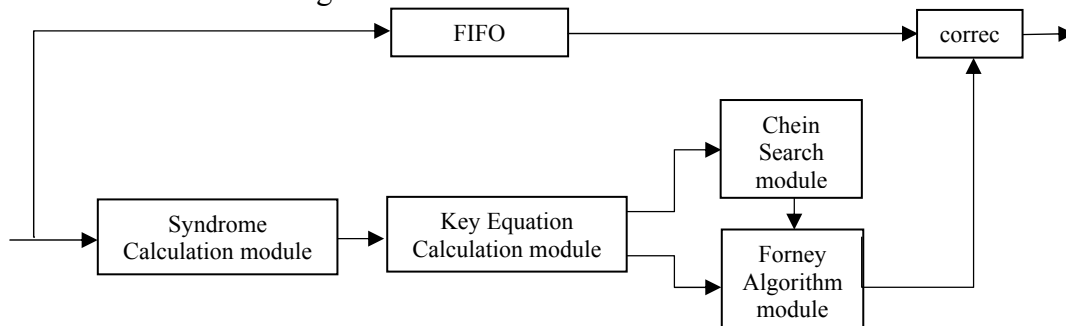


Fig. 3 RS codes decoder schematic diagram

## Main Module Design and Simulation

At the decoder side, the syndrome calculation (SC) module can be implemented by GF(2<sup>8</sup>) multiplier with constant coefficients and shifting register, as indicated in [6]. Calculation formulas is

$$S_i = R(\alpha^i) = \sum_j r_j \cdot \alpha^{ij}, i = 0, 1, 2, \dots, 2t-1, j = 0, 1, \dots, n-1. \quad (5)$$

The structure of SC module is shown in Fig. 4.

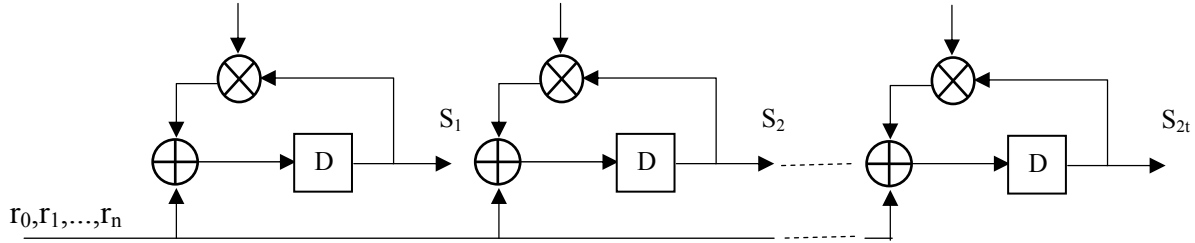


Fig. 4 SC module schematic diagram

The key equation calculation (KEC) module is the key of RS codes decoder, it determines the performance of the decoder. Moreover, this module is the most complicate and time-consuming section. Thus we choose BM algorithm. Because it has shorter iterative path. Usually, we need use RiBM algorithm to eliminate the inverse operation in the algorithm, explained in [7]. This algorithm has regular structure and low hardware complexity.

The *Chein* search (CS) method was proposed in 1964. It is a practical method to search the root of error position polynomial. The structure of *Chein* search method is shown in Fig. 5.

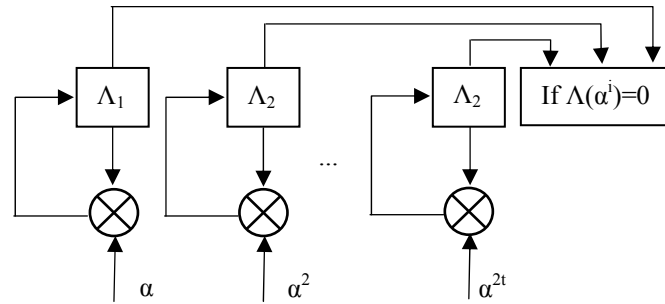


Fig. 5 CS module schematic diagram

The error value is calculated by Forney equation, see [5].

This VLC system is used to simulate source information which has been scrambled, encoded and interleaved, then sent it to transmitter and then reach to an optical receiver over AWGN channel. The decoder is based on RS (204,188) code, with rate 0.92, the error correcting capability equal to 8. The VLC system simulation based on soft QUARTUS II 9.0. The simulation of main modules is shown in Fig. 6:

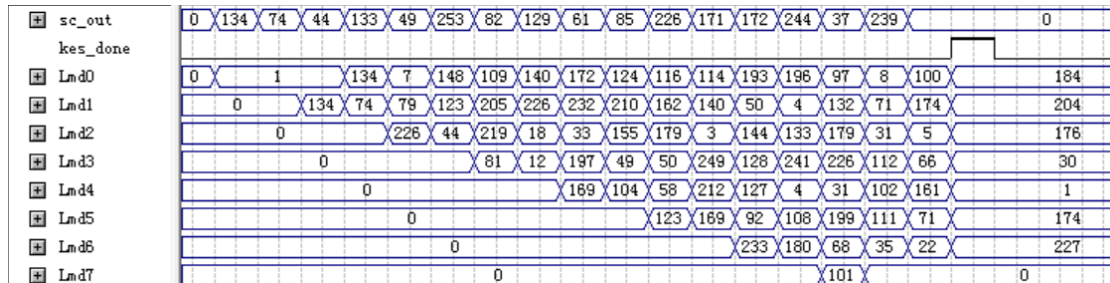


Fig. 6 KEC module simulation result

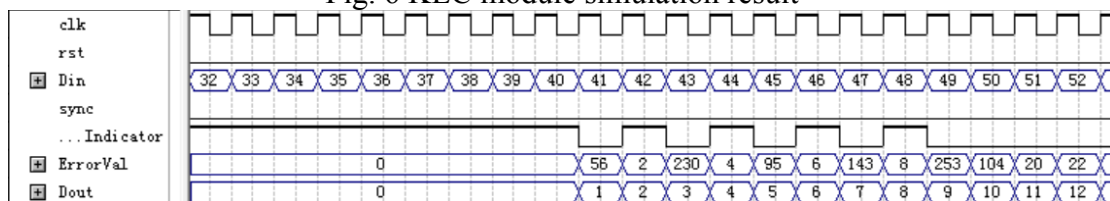


Fig. 7 Chein Search and Forney algorithm simulation result

The results is shown in Fig. 7. Pin Err\_Indicator shows four position of errors and pin ErrorVal displays the corresponding values of four positions. The decoder output (Dout) is equal to input (Din) as we can see from Fig. 7. It shows that the RS codes decoder can apply in VLC system.

## Summary

In this paper, a channel coding scheme for Visible light communications was proposed. We designed and implemented the encoder and decoder of RS (204,188) to anti the burst errors. The decoder was designed with pipeline structure and multipliers over  $GF(2^8)$ , which could occupy less hardware resources on FPGA and yield a significant throughput improvement. In future work, if the LDPC codes were applied as the inner codes of the serially concatenated scheme to deal with random errors and the RS codes were applied as the outer codes to anti the burst channel loss, the VLC system performance would be improved better.

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