A Novel Integrated Testing Platform Based on Open VPX

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Abstract. With the development of high-speed and real-time signal processing systems toward modularization, generalization and reconstruction, a method of modular design has been proposed and accepted widely. However, the increasing module types and extending production scale make the module-test challenged and the test results of modules are dispersed, which make it difficult for collection and post-maintenance. Moreover, it's difficult to perform traversal test with so many module-combinations, and this consumes excess equipments and human resources. In this paper, we proposed a concept of integrated testing, and designed a integrated testing platform (ITP) based on the Open VPX architecture. The ITP can achieve intelligent identification and resources detection of the under-test single/multiple modules after startup, and with the users' manual configurations, the ITP can then perform the traversal test automatically. Besides, the ITP provides functions such as real-time fault alarm and the test report printing. The ITP has been applied in mass testing for an Open VPX-based high-performance processing module, with multiple VLSI (Very Large Scale Integrated) circuits integrated, such as TI TMS320C6678, Xilinx Virtex-6,etc, and greatly increases its efficiency and accuracy.

1 Introduction

With the increasing diversity and complexity of electronic equipments, more and more rigorous test are required before market, and this makes automatic test become critical needed[1]. Currently with the development of high-speed real-time signal processing system, the traditional customized test method has shown its shortcomings, such as occupying excess resources, slow updates, upgrade difficulties, etc. As a result, a novel test methodology is necessary to satisfy the increasing test demand, especially for the high-speed real-time signal processing systems adopting modular designs.

Module independence is the keystone of the modular designs, including functional independence and structural independence, and this makes it easy to implement the development of divided software. With traditional test method, a large-scale embedded software system can be divided into several related smaller testing-task, which can be encoded by separate programmers simultaneously. And we then can test these modules one by one after coding work. However, as modular design method allows high-speed real-time signal processing system to reconstruct a product rapidly, the traditional method of dispersed test limits the test or maintenance efficiency and increases the product period to the market [2].

In this paper, we proposed a concept of integrated testing, which focuses on mass test intelligently and automatically. With the idea, we designed and implemented an Open VPX-based

integrated testing platform (ITP), which allows single or multiple modules test simultaneously. The ITP makes up the deficiency of the traditional methods, and makes it effective and accurate to test high-speed real-time signal processing system based on Open VPX [3]. Besides, the ITP supports real-time fault alarm and test reports printing, which helps to setup the archives for tracking back. The ITP has been applied in multiple high-speed real-time signal processing systems, it's validated that, it greatly improves the test efficiency and completeness, reduces equipment and labor costs, and this offers a valuable reference to the development of the automatic testing technology.

The paper is arranged as follows. Section II introduces the signal processing system based on Open VPX including its architecture and physical resources, and demonstrates its ITP. Section III describes some of the key technologies of integrated testing such as test flow control, traversal test, interface, etc. Finally section IV concludes the paper.

2 Integration Testing Platform based on Open VPX Architecture

2.1 Brief Introduction of Open VPX

The Open VPX is a architecture standard issued by the VITA organization, and it has three advantages: fast-integration through standardized backplane and system architecture, reasonable estimating for modules interoperability and easy to implement module upgrades [3]. The current international mainstream system architecture standards are the CPCI and Open VPX. The platform based on Open VPX architecture is superior to the platform based on CPCI architecture in the high-speed transmission of backplane connectors, interconnection and so on [1]. In addition, the Open VPX supports strong I/O capability and high performance network switching capability by employing advanced switch network interconnection technology such as Rapid IO (SRIO), PCI Express and other high-performance interfaces. The signal processing system based on Open VPX architecture standard can adapt to the various complex process-driven modes such as parallel mode, multiple data streams and types, etc. And this brings two characteristics: hybrid parallel structure and multi-level interconnection structure. The Open VPX architecture utilized bus, point-to-point switching and synchronous timing network interconnection structures. These three complementary and orthogonal interconnection structures can separate data streams of low-speed, non-real-time, high-speed, real-time, and can provide strict synchronization to each module [3].

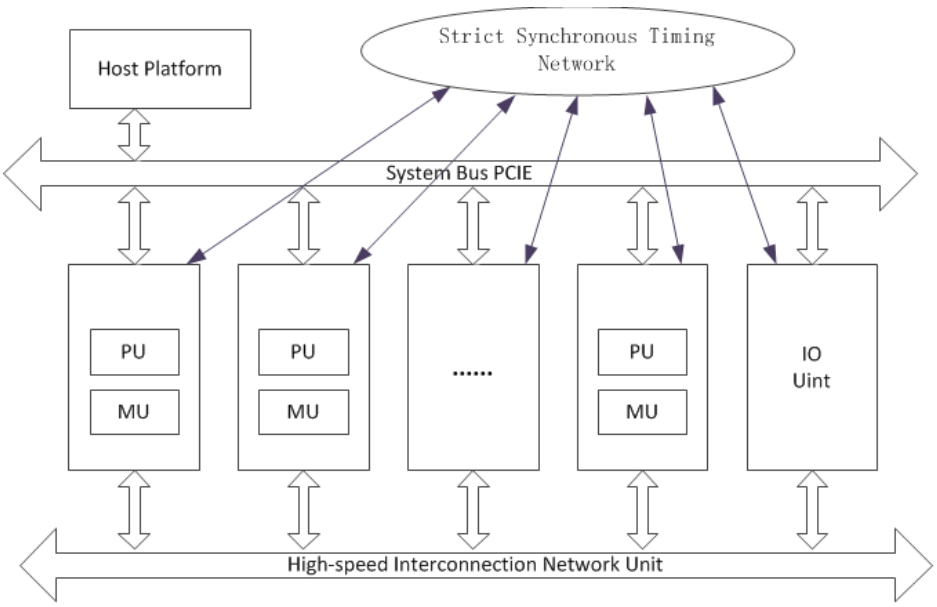

Figure 1: Signal Processing System Architecture Model Based on Open VPX

To satisfy the demand of real-time information processing, we proposed a real-time signal processing architecture based on Open VPX standards, by combining the characteristics of Open VPX standard and parallel processing system architecture. The architecture is scalable, reconfigurable, strong real-time and parallel processing, and its system architecture model is illustrated in Figure 1. As can be seen, it's composed of the processing module IO module, bus interconnection network, configurable switched high-speed network and strict synchronization and timing network.

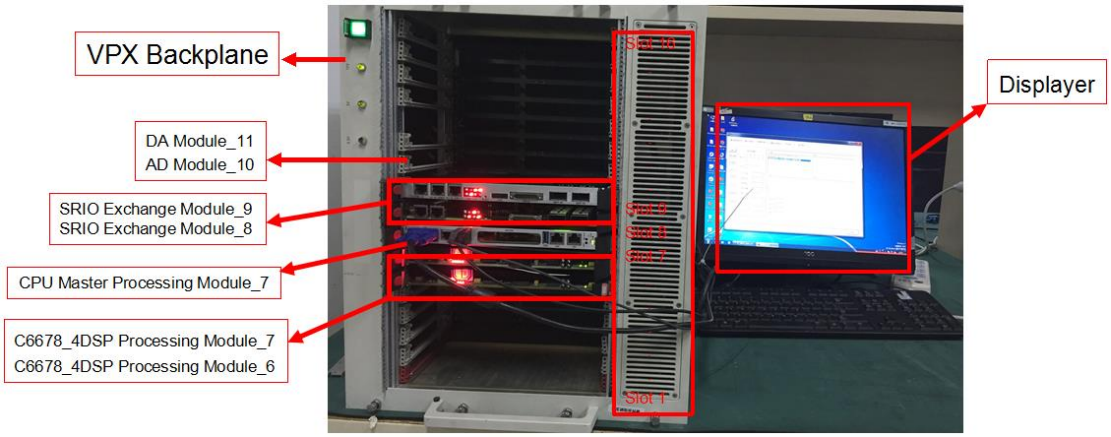

Figure 2: Slot Distribution of Signal Processing System Based on Open VPX

As a high-speed real-time signal processing system, it generally includes a master, ADC/DAC, exchange, processing, storage and other modules. The master module manages the entire system resources, monitoring and scheduling, the ADC / DAC module finishes the data acquisition and playback, and the exchange module serves as the route of data flow. The processing module performs the signal processing algorithm. The storage module stores the original and post-processing results [3].

In this paper, the integrated testing platform sets up a real-time signal processing system, which employs Open VPX structure with 16 slot backplane interconnect as illustrated in Figure 2. It includes 14 load slots and 2 switching slots and the adjacent load slots employ PCIE and Rapid IO for high-speed data interconnection. All the load slots share FPDP (user defined) and synchronization (SYNC) bus to achieve inter-board control information transmission and synchronization. The slot 7 is the master slot to implement the master control of the test platform, slot 8,9 are exchange slots, and the boards located on other load slots are the objects under test.

The signal processing system based on Open VPX architecture standard provides a fundamental system for the integrated testing platform to bring its superiority into full play.

2.2 C6678_4DSP Board Applied to Integration Testing Platform

As aforementioned, the ITP can test all the board located on load slots except slot 7, and it has been used to test C6678_4DSP_SD board, C6678_4DSP_VPX board and C6678_4DSP_ZD board. Here we take a high-performance processing module C6678_4DSP_VPX to demonstrate the ITP. The diagram of the module is illustrated in Figure 3.

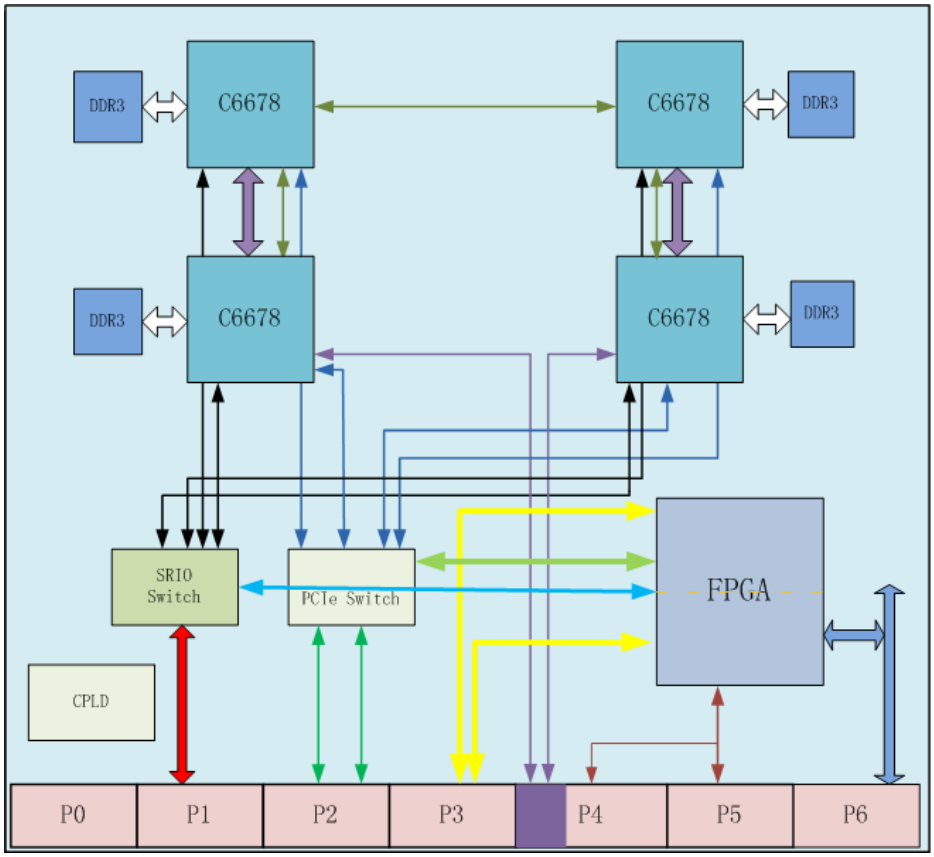

Figure 3 :C6678 General Signal Processing Module Block Diagram

It includes physical resources as follows. Four TMS320C6678 from TI are integrated, whose operating frequency is up to 1.25GHz, and the four C6678 are virtualized as a processing node by serial Rapid IO. Of which, DSP0 and DSP1, DSP2 and DSP3 are paired to be virtualized as smaller processing nodes by Hyperlink. As the external storage, single C6678 can support 2GB \ 4GB \ 8GB of DDR3 with operating frequency of 1333MHz or 1600MHz. Each C6678 and FPGA realizes a 4X SRIO which supports 2.5Gbps, 3.125Gbps, 5.0Gbps per channel via Rapid IO Switch. Each C6678 realizes a 2X PCIE which supports 2.5Gbps and 5.0Gbps per channel via PCIE Switch. FPGA realizes point-to-point serial interfaces through backplane such as Rocket IO, link, PCIE and Rapid IO. The CPLD monitors the status and realizes the board reset, configuration and other functions.

The proposed ITP can realize the automatic traversal test to the module resources including PCIE bus, Rapid IO bus, Hyperlink, FPGA, SPI Interface, EMIF interface, DDR3 memory, etc. It can be used for development, debuging, maintenance, fault diagnosis, etc, and can greatly improve the efficiency and accuracy. Besides, it can support testing multiple modules simultaneously, and this makes it flexible for the user to control the testing environment parameters and get results.

3 Key Technology of Integration Testing Platform

3.1 Integration Testing Process Flow

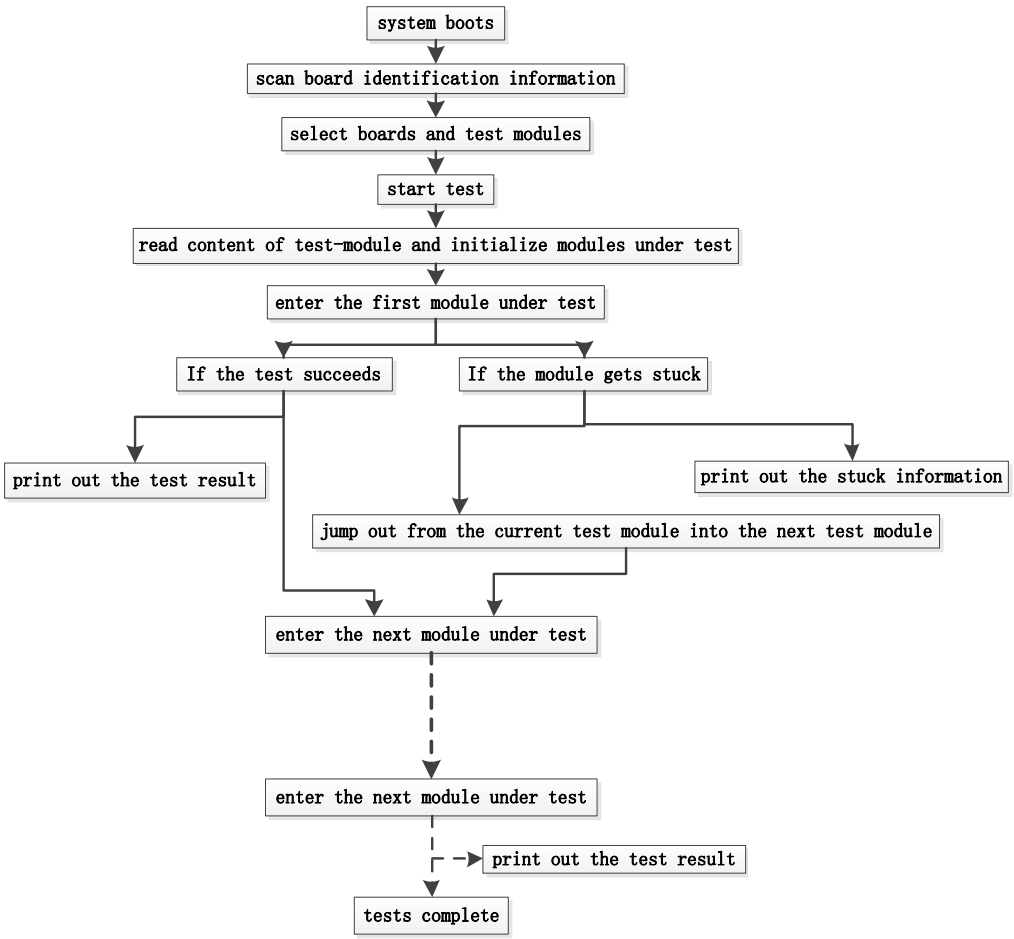

Figure 4: Open VPX Integrated Testing Platform Testing Flow

In the ITP, all the modules under test (MUT) are controlled and scheduled by master machine uniformly, and this provides the physical basis for the platform [4]. As illustrated in Figure 4, the master machine communicates with the target module via PCIE bus during the entire testing process.

The first is the interactive feedback between the master machine and the MUTs. The master machine obtains the basic information about the MUTs such as the system name, module name, number of modules, module versions and so on, which is located in a specialized register of modules. During the identification process, the resources of the modules, called test-module, can be chosen optionally, which will be added into testing sequence automatically. During the testing processing, the master machine will read the content of test-module, and initialize the MUTs for step-by-step testing. After the completion of the work mentioned above, the ITP enters the first MUT. If the test succeeds, the master machine will print test result information. And the ITP will enter the next MUT [5]. Besides, we also add a timer in the test module easy to get stuck, so if the test gets stuck, the master will jump out of the current test module into the next test module and print the stuck information once beyond the normal working time [5]. According to the above test procedure, the ITP will complete all the testing of MUTs gradually.

During the test, the master machine can monitor the test process and show the real-time test results feedback in the screen interface, and finally can summarize results to form a complete test report.

3.2Traversal Module Testing

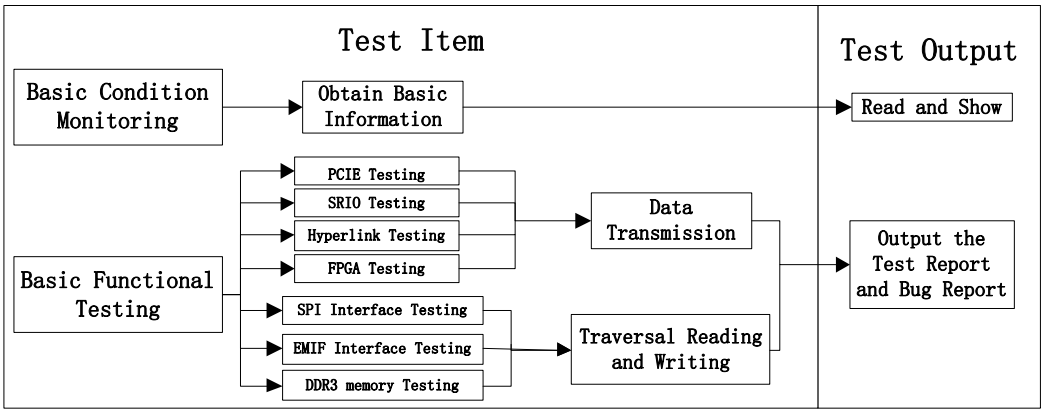

Figure 5: Processing Module Test Block Diagram

In order to realize traversal test, the ITP employs a effective test framework with proper data stream control. We divided the MUT into the following two sections: basic condition monitoring, basic functional test including PCIE bus, Rapid IO bus, Hyperlink, SPI Interface, EMIF Interface, DDR3 memory. For the basic condition monitoring, the master machine obtains the module name, version, production date and other information by reading module-specific EEPROM, and meanwhile, it also monitors power supply, clock, temperature and other module status information by reading the FPGA status register and updates them in real time, and alarm the tester or sent a emergency reset. The basic functional test is divided into one-click automatic test and manual test. The former tests all the physical resources of modules automatically according to the prebuilt framework and data stream, and the printed report will include whether all the physical resources functions are normal or not and whether the target performance indicators are eligible or not. The latter tests certain physical resources specified by user, which can help for debugging and fault diagnosis.

3.3 Human-computer Interaction Interface

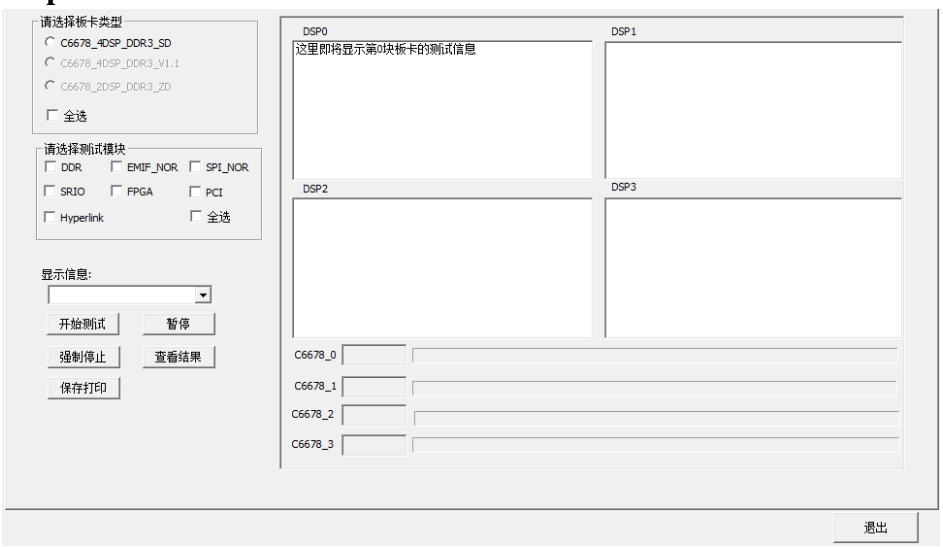

Figure 6: Human-computer Interaction Interface

The interaction interface is concise and intelligent as shown in figure 6. Test control buttons include "Start Test", "Pause", "Force Stop", "Save" and "Print and View results". The test procedure is that first we select the targeted test board and test module and then click on the "Start Test" button. Test information is displayed on display frames and four display frames show four DSP test information respectively. There are also four progress bars to report the progress of each DSP.

Figure 7: The Output Interface of FPGA Testing

In figure 7, FPGA testing is taken as an example. We can see that there are six C6678_4DSP_VPX boards in the case and the real-time test information of the first board is displayed on four display frames respectively. Four progress bars report the progress of each DSP. The bandwidth and other test results will print out ultimately. FPGA testing is successful, so the ITP enters the next MUT and print out the information of the next testing module. If the FPGA testing fails, the ITP will print out the information "FPGA testing failed. " and enters the next MUT. After all the MUTs have been tested, the ITP will print out the overall test results.

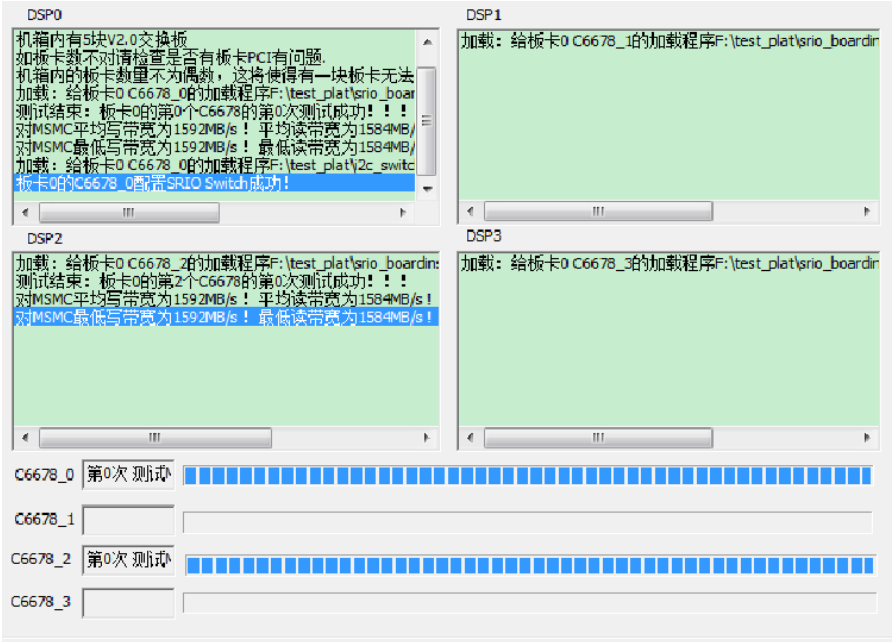

Figure 8: The Output Interface of SRIO Testing

In figure 8, we select the certain DSP0 and DSP2 to do SRIO testing. The display frames and progress bars display information of DSP0 and DSP2 only. We can select the certain DSP and modules for testing based on different demands. Through experiments, we can find that the integrated testing are more intelligent, efficient and easier than the separate module test.

4 Conclusions

In this paper, we propose a integrated testing platform (ITP) with characteristics of intelligent and automation It realizes traversal test for various functional connectivity and the key indicators of system. Moreover, it offers a friend interface to user, and supports convenient functions such as real-time fault alarm and the test report printing. It reduces costs, improves test efficiency and shortens the development cycle of the system, especially for those requiring mass testing. As is validated in mass testing of several real projects, besides the convenient operation, the ITP can greatly increase efficiency and accuracy of the test.

Acknowledgment

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