The Application of Equal Precision Frequency Measurement Technology in Motor Speed Measurement System Based on CPLD

Hui Li[1, a, *] and Jing Li[1]

[1]Faculty of Automation, Huaiyin Institute of Technology, HuaiAn 223003, China

[a]lijing_1981_312@163.com

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Abstract. In order to increase the motor speed precision and accuracy, this article presents a equal precision frequency measurement technology based on CPLD, as well as for analog glitch generated from encoder vibration and other factors, digital low-pass filter based on the state machine is designed, and finally the design is simulated on Quartus II software platform and verified on the hardware platform.

Introduction

Frequency measurement is one of the most basic measurement technology in the field of electronic measurement, frequency measurement current main includes four kinds of implementation way, such as direct counting, period measurement method, mixed measurement and equal precision frequency measurement. The first is a direct counting method, which has big measurement error at low frequency, usually is used for high-frequency measurements. The second way may produce big error when the test signal frequency is high, Thus this way is usually used for low frequency measurement; The third method is a combination of the first and the second methods, namely the first way is used for high frequency measurement and the same time the second way is used for low frequency measurement. This method can make up for deficiencies in the methods described above to some extent, but it is difficult to determine the best points measuring point, and its circuit is very complex. The fourth is equal precision frequency measurement method. The measurement error using equal precision frequency measurement method herein does not vary with the frequency of the measured signal varies[1]. The design is complete using VHDL language. There is hardware connection between the motor shaft and the encoder. Thus mechanical vibration will be produced when the motor is running, resulting in the output of the encoder signal randomly generates a lot of high-frequency glitches, easy to count malfunction, which will affect the accuracy of speed, therefore, the signal must be filtered before entering the speed module. The hardware filtering is easy to implement, but the filter is inaccurate, and easy to filter the useful signal. And the same time the software filter is usually affect the speed. But CPLD uses parallel processing architecture, so its running speed does not affect only part of the expense required resources. Therefore, digital filtering effect using CPLD is good if the resource can be permit. So digital low-pass filter based on state machine is designed in this paper.

Overall System Design

System mainly consists of two modules, namely: digital filtering, and equal precision frequency measurement. Specific module is shown in Fig. 1.

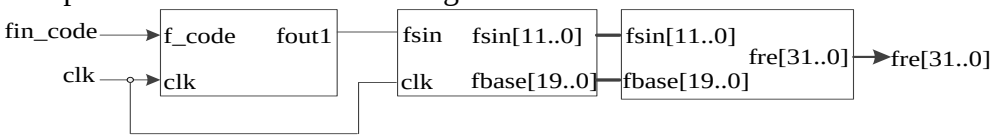


Figure 1. The frequency measurement module diagram

Wherein fin_code is a single-phase pulse signals from the incremental circle grating encoder, clk is the system reference clock signal (50MHz), fre [31..0] is synthesized signal after low-pass filtering and equal precision frequency measurement processing. The foremost give in Fig. 1 is all-digital low-pass filtering sub-module based on the state machine, the middle is equal precision frequency measurement control module, the last is data synthes module.

Sub-Module Design

Digital Low-Pass Filter Design Based on State Machine. In consideration of the encoder output signal in experiment is not higher than 30Khz, so choose a cutoff frequency of 30Khz. And the pulse width of the 50% duty cycle signal is about 15us. After a lot of observation and analysis shows that: the interference signal output from the encoder of the system are mainly two: positive and negative interference, frequency interference signals between 30Khz-50Mhz. It is considered that the pulse width of signals below 15us are all interference. And it was not be count if the signal is interference signal when the speed is measured. Specific design state diagram is shown in Fig. 2.

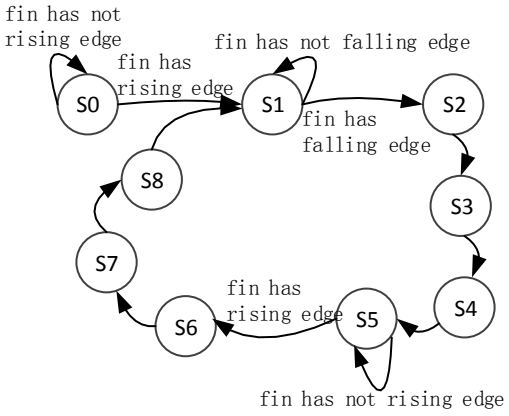


Figure 2. Digital low pass filter module state ASM diagram

Among them:

S0 represents the initial state, receiving an external input signal to be filtered named fin, the count value is cleared, stop counting; S1 state represents that timer is started; S2 state represents loading time control signal and stopping count; S3 state represents that detection timing time is less than 15us or not, if less than 15us, the signal may be considered the interference signal, otherwise generating high level; S4 state timer value can be to zero;S5 state starting a new round of time, and clearing time load signal; S6 state stopping count and generating new time load control signal; S7 state represents that detection timing time is less than 15us or not, if less than 15us, the signal may be considered the interference signal, otherwise generating low level; S8 state clearing count value.

The design of equal precision frequency measurement sub-module. The equal precision frequency measurement is used in speed measurement module. And the frequency measurement accuracy are controlled by a preset threshold and the measured signal[2,3]. 50MHz clock is adopt as Cpld master clock. The precision of measuring only associated with the frequency and voltage stability degree of reference signal, and has nothing to do with the frequency of the measured signal

So can ensure that measuring accuracy remains the same throughout the measurement frequency, it is within the period of guarantee the main motor in different speed can keep the same speed measuring precision.

1ms is selected as speed test period. The threshold signal generated by Cpld is synchronized with the measured signal. Cpld control reference signal and measured signal count at the same time, send Dsp two count values which is calculated to obtain a value of the measured signal frequency. The measured signal frequency can be expressed as the Eq.1.

$$f_x = \frac{N_x}{N_s} \times f_s \quad (1)$$

Wherein fx representative of the measured signal frequency, fs on behalf of the reference frequency(50MHz), Nx is of the number of measured signal pulses counted within one millisecond, Ns representative of the number of pulses of the reference signal within one millisecond counts.

There is Eq.2:

$$\frac{\Delta f_x}{f_x} = \frac{\Delta N_x}{N_x} - \frac{\Delta N_s}{N_s} + \frac{\Delta f_s}{f_s} \qquad (2)$$

From Eq.2: If you ignore frequency accuracy error of the reference signal fs, The relative error of the frequency measurement of the system is only related to the positive and negative 1 errors generated by fs, which is not related to the frequency of the measured signal. The measured signal is about 30kHz output by the encoder signal after low-pass filtering(fold into speed at around 1000r/min or so). Therefore measured signal frequency value accounted for 1.5 bytes, the frequency of the reference signal value accounted for 2.5 bytes.

Hierarchical design[4,5] module chart of the equal precision frequency measuring module is shown in Fig. 3.

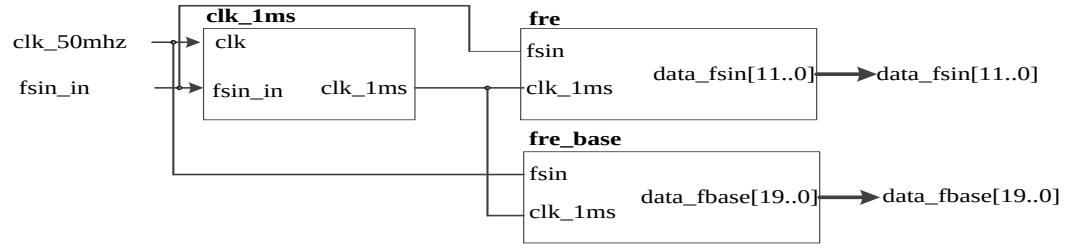


Figure 3. The equal precision frequency measuring top module

In Fig. 3, clk_1ms module is used for generating a 1 millisecond synchronization threshold signal, fre module is frequency measurement module for measured signal, and fre_base module is frequency measurement module for base signal. Graphical text hybrid design is adopt in the whole design. The top-level design uses graphical style which is concise and clear, and the Bottom-level design uses text style. Component Instantiations is used for calling sub module. The design of entity is described as follows:

```
Entity freq is - a substantial portion of Frequency Measurement Module
port (fsin, clk: in std_logic; - define the input port
data_fsin: out std_logic_vector (11 downto 0));
End entity freq;
The structure is described as follows:
Architecture bh of freq is
component Cnt10
…
end component;
signal TSTEN: std_logic; ---- the definition of the control signal
...
BEGIN
   U0:TESTCTL PORT MAP(CLK=>CLK,TSTEN=>TSTEN,
   CLR_CNT=>CLR_CNT,LOAD=>LOAD);
   U1:CNT10 PORT MAP(CLK=>FSIN,CLR=>CLR_CNT,ENA=>TSTEN,
   CQ=>DIN (3 DOWNTO 0),CARRY_OUT=>CARRY1);
   …
   U:REG12B PORT MAP(LOAD=>LOAD,DIN=>DIN(11 DOWNTO 0),DOUT=>DATA);
END;
```

Simulation Test of Equal Precision Frequency Measuring Module

In order to verify the system function, the simulation of the equal precision frequency measuring module are finished on QuartusII software platform in this paper. And there are five frequency points(1KHz, 5KHz, 12KHz, 15KHz, 20KHz) in 0 to 30KHz which would be simulated. The simulation time of 1 second, and specific simulation waveform is shown in Fig. 4.

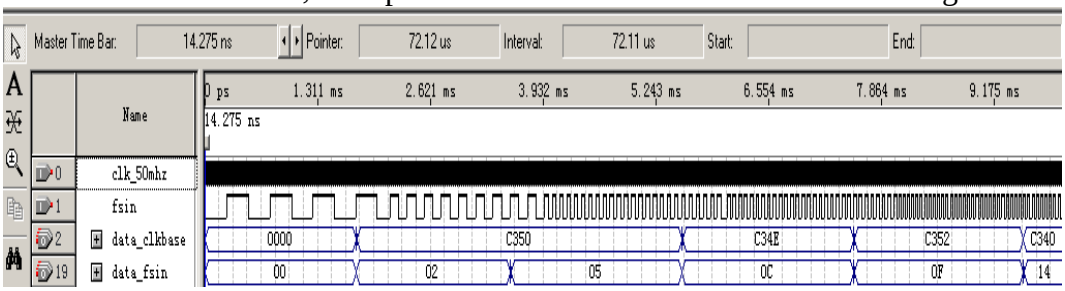


Figure 4. Equal precision frequency measurement module simulation map

In Fig. 4, clk_50mhz is the main crystal(50MHz), and the same time it is the base clock of the equal precision frequency measurement module. In addition,fsin is the main motor encoder output signal after processed by low-pass filter. Data_clkbase is the count value of the reference clock within the gate time. Data_fsin is the count value of the measured signal within the gate time. After simple calculation frequency test results of 5 frequency points can be obtained in Table 1.

Table 1 The test frequency and test precision of different frequency point.

actual (KHz)	frequency	2	5	12	15	20
testing (KHz)	frequency	2	5	12.00048	14.9994	20.0064
error		0	0	+0.004%	-0.004%	+0.032%

It can be seen from the test data in table1 that test accuracy of each test point is above 0.05%. Thus, the measurement accuracy can meet the design requirements of the system.

Simulation of Full Digital Low Pass Filtering Performance Based on State Machine

The simulation about full digital low pass filtering performance is finished on QuartusII software platform. The simulation result is shown as Fig. 5.

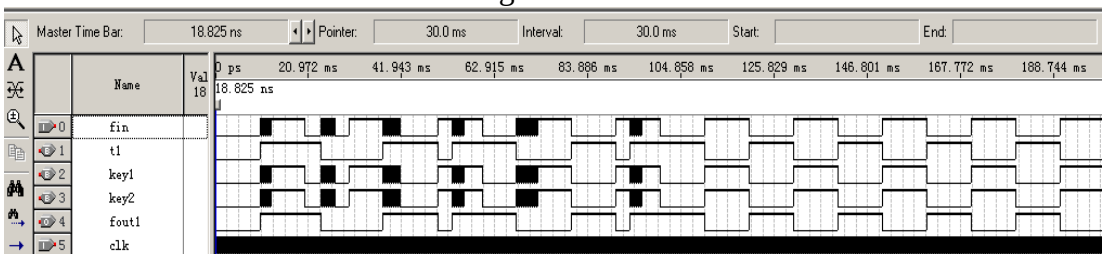
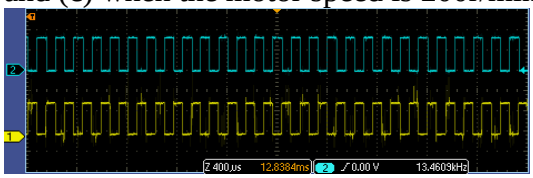


Figure 5 The full digital low pass filter module simulation curve

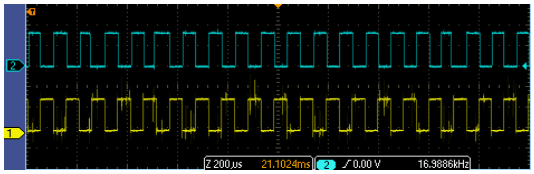
The simulation time is 200 milliseconds. As can be seen from Fig. 5: The input signal is a high frequency pulse signal composed of 50KHz High frequency pulse jamming signal and 50Hz signal. There is same pulse number in fout1 which is obtained after filtering and the base frequency signal. Thus, from the point of view of the counting frequency, the frequency of fout1 and 50Hz signal have the same frequency, to a certain extent, it can achieve the function of low pass filter.

Experiments of Full Digital Low Pass Filtering Performance Based on State Machine

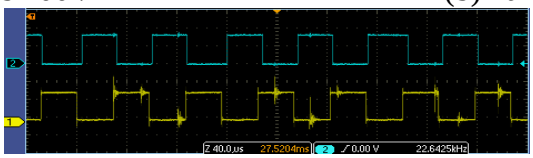
Finally, experiments of full digital low pass filtering performance based on state machine is finished. And the output signal waveform before and after filtering are shown on oscilloscope as Fig.6 (a),(b) and (c) when the motor speed is 200r/min,300r/min and 500r/min.



(a)main motor speed is 200r/min



(b)main motor speed is 300r/min



(c)main motor speed is 500r/min

Figure 6. Digital filtering effect comparison chart

The above signal in Fig. 6 is encoder output signal after filtering, and the follow signal in Fig. 6 is the signal before filtering. As can be seen: After the full digital low-pass filter processing, Burr signal can basically be filtered. Due to the state machine processing and determination takes time, the signal after filtering is lag of 90 degrees or less in phase than the original signal. Because that the system uses equal precision frequency measurement, gate signal synchronized with the measured signal, so long as the proper phase compensation based on the measured signal to the main motor speed does not substantially affected.

Conclusion

The simulation and experimental verification, sum up: the frequency test accuracy of equal precision frequency measurement is 0.05% or more. And the all-digital low-pass filtering function can be successfully achieved in the system, fully meet the need of the speed measurement.

Acknowledgement

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