The Development of Speed-Tension Type Three-motor Coordinate Synchronous Control Platform Based on Multi-microprocessor

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Keywords: Real-Time; Multi-Microprocessor; Coordinate Synchronous Control; Overshoot

Abstract. In order to improve the traditional speed-tension type three-motor synchronous control platform based on PLC bus control to further enhance the speed and control accuracy of the control system, enhance the control effect, Speed-Tension type Three-motor coordinate synchronous control platform based on Multi-microprocessor is proposed in this paper. In this platform, the complex programmable logic devices (CPLD), Digital Signal Processor (DSP) and microcontroller (MCU) are combined. In order to improve rapid and synchronization of the control system, CPLD Parallel nature is used to achieve three serial ports synchronous and concurrency control; Complex control algorithms are implement by the use of DSP fast and efficient data processing capabilities; Experimental results show: The control system is stable, at the same baud rate the control speed of the platform based on multi-microprocessor is more than three times faster than the one of the traditional PLC bus control platform. In the multi-microprocessor control platform， under the same control algorithm regulation time is more fast 0.53 seconds than traditional PLC control platform, the overshoot of the system is 13.53% of the one using traditional PLC control platform, and the tracking the maximum error reduces 60.53% than the one of the traditional PLC control platform.

Introduction

With the development of modern industrialization, the application of multi motor synchronous coordinated control is more and more widely, for example, in the textile, papermaking, printing and dyeing industry[1]. With the development of intelligent information technology, higher requirements have been put forward for real time control of multi motor synchronization control system. The traditional multi motor system is often uses bus polling control control, long period, poor real-time control, has been unable to meet the three motor and multi motor synchronous system requirements; The three motor synchronous control based on traditional PLC bus control is proposed in the [2-4]. Respectively on the system dynamic performance, steady state performance and decoupling performance are studied by experiment and analysis, control system is stable, but there are some overshoot, tracking steady error exists; The control platform of in this paper uses multi microprocessor as control core, using CPLD hardware synchronization control features, improve the adjustment time, reduce the overshoot To improve the tracking accuracy and decoupling performance of the system, so as to improve the control performance of the whole control system. Synchronous control scheme is proposed by the example of the speed - tension type three motor synchronous control system adopting CPLD multi RS485 bus synchronization control mode. The real-time in equal communication baud rate control can be increased more than three times. So the new hardware control platform for the speed - tension type three motor synchronous control system is developing.

In this paper, we first introduce the framework of the overall design of the system, discussed the design of each sub module, for CPLD part by top-down modular design scheme [5]; Then the communication speed of the control platform and the traditional PLC bus control platform are compared with the test. In the hardware experiment control platform square wave tracking performance are tested using the first-order fuzzy immune active disturbance rejection control strategy, and the control effect on the traditional PLC bus control platform are analyzed and compared.

Platform Overall Design

The system is composed of CPLD control module, DSP control module and so on. System structure diagram is shown in Fig. 1.

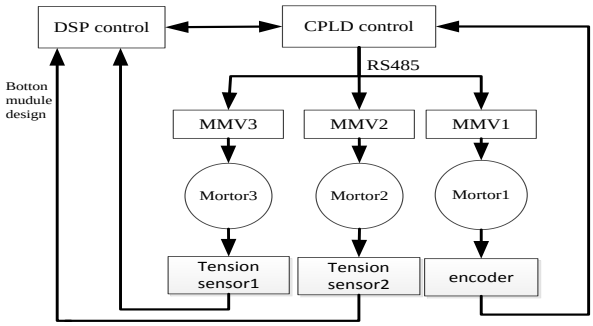


Figure 1. whole framework of system

Each Sub Module Design

CPLD Top-Level Module Design. The top-level design mainly includes frequency measurement module, display module and communication module. The top-level module is shown in Fig. 2.

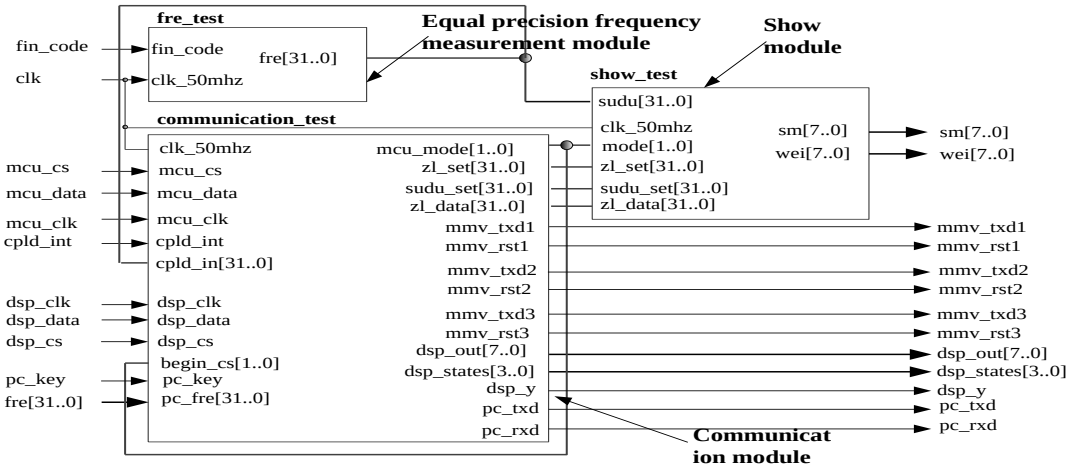


Figure 2. The framework of CPLD part

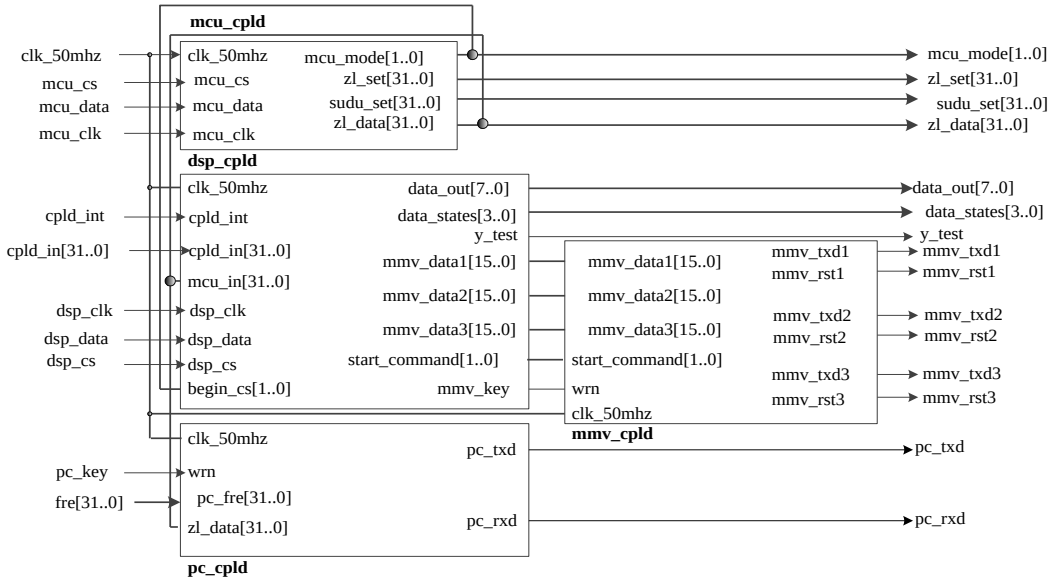


Figure 3. Communication module diagram

CPLD Middle Layer Module Design. Each module corresponds to the top level file carries on, is an independent design unit, independent simulation debugging, referred to here as the middle layer module. According to Fig. 2 shows that the system includes frequency measurement, display and communication module three intermediate layer.

Communication Module. The communication module can be divided into SPI communication module (mcu_cpld) with MCU, RS232 communication module (pc_cpld) with the PC, data communication control module between CPLD and DSP(dsp_cpld), and RS485 converter communication module(mmv_cpld), specifically the module graph is shown in Fig. 3.Mcu_cpld module is used for communication between CPLD and MCU. Dsp_cpld module is used for communication between CPLD and DSP. And this module is compose of two parts: the one is a module which sends data to DSP. Another is a module which receives data from DSP by SPI style. Mmv_cpld module is used for control three inverters in the style of multi-RS485 bus. In this module, mmv_txd1, mmv_rst1, mmv_txd2, mmv_rst2, mmv_txd3, mmv_rst3 are respectively control signal for controlling the speed of the main motor, the tension1 between the main motor and the second motor, and tension2 between the second motor and the third motor. Pc_cpld is a communication module for PC.

Display Module. The display module can be divided into frequency division module of the driving signal, digital display module. The design is a conventional design method, so here is no longer mentioned.

Frequency Measurement Module. Equal precision frequency measurement method is adopt in this paper. And the design is a conventional design method, so here is no longer mentioned.

The Design of DSP Control Module. Due to the characteristics of the DSP chip itself, DSP control in data processing has the advantage of greater than general CPU. Here the DSP control module is mainly responsible for algorithm design, color screen control and communication function with CPLD. Where the first-order fuzzy immune active disturbance rejection control algorithm is adopt, and fuzzy immune active disturbance rejection control is the combination of the modern fuzzy immune algorithm and active disturbance rejection control algorithm, which has strong anti-interference ability, good robustness , response speed and many other advantages. The main stream is shown in Fig. 4.

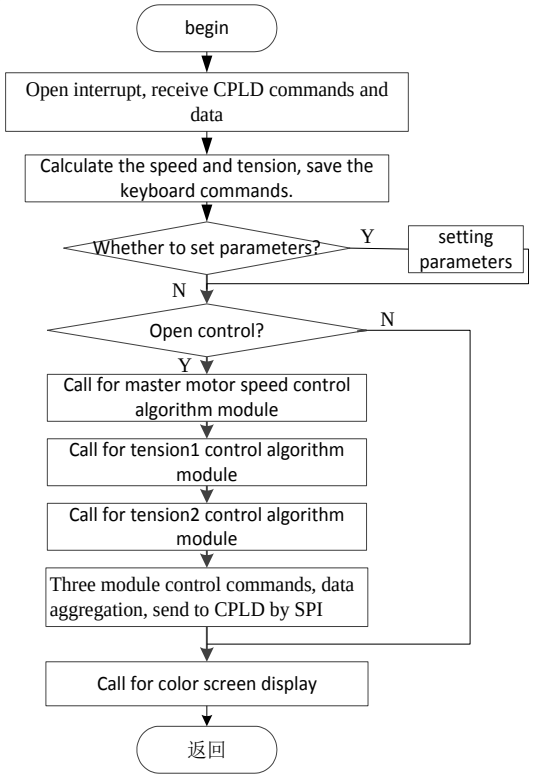


Figure 4. DSP main Flow chart

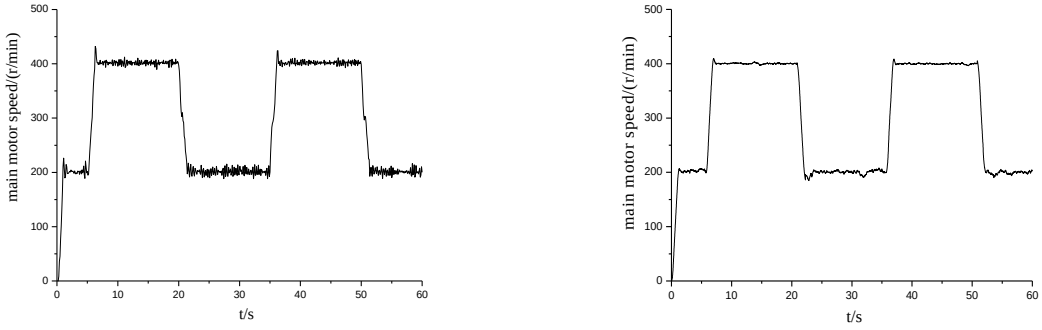
As can be seen from Fig. 4, the DSP receives command and data from the CPLD module in the style of interrupt, after calculation and detection of control commands, and then call the three corresponding algorithm module, and summary to CPLD driving multi-RS485 bus for controlling three inverters work at the same time, last call screen driven color curve display.

Experiment and Analysis

Three three-phase AC asynchronous motors is used as the control object in the experiment. The rated motor speed is 1494r/min, inverter is Siemens inverter, the processor selects DSP2812 microprocessor and CPLD uses chip MAXII EPM1270TC5 and speed sensor uses incremental 2048 reticle circle grating encoder, the tension sensor selects SL-100.

Comparison test of Main Motor Square Wave Tracking Performance. The first-order fuzzy immune active disturbance rejection control algorithm is adopted on two kinds of control platform for square wave tracking performance test, the traditional PLC control platform control cycle T=100ms. According to the numerical simulation of ESO show that, the parameter β_{i1}, β_{i2} are determined by the sampling step, including: $\beta_{i1}=1/h$, $\beta_{i2}=1/(5\times h^2)$. Take h=0.1 seconds, so β_{i1}, β_{i2} were selected as 10, 20. Corresponding to the control platform, the sampling control cycle increased by ten times, T '=10ms, therefore, β_{i1_1}, β_{i2_1} were selected as 100, 2000.

The speed reference signal is a standard square wave signal which is 200r/min to 400r/min, and testing time is 1 minute. The main motor tracking the square wave signal on the traditional PLC control platform and the multi microprocessor control platform, tracking curve is shown in Fig.5 (a), (b).



(a) Traditional PLC platform control (b) Multi microprocessor experimental platform

Figure 5. Square wave tracking performance test curve

A list of the performance parameters of the square wave tracking is shown in Table 1.

Table 1 of square wave tracking performance under two different control platforms

Performance index	control platform	
	traditional PLC control platform (T=100ms)	multi microprocessor control platform (T=10ms)
Adjust time/s	1.6	1.07
overshoot/%	12.05	1.63
Maximum steady-state error /(r/min)	20.90	8.25

From Table 1 with Fig. 5 shows: using the control platform (experimental platform based on multi processor) can greatly improve the control performance of the control system, in the dynamic performance of regulator system time than the original PLC control platform fast 0.53 seconds, the system start-up overshoot greatly to damp, the overshoot of system of the experimental platform is the traditional PLC control overshoot of 13.53%, compared to the traditional PLC control platform

to the system overshoot has been reduced nearly 7 times, in the steady state behavior of the system, tracking the maximum error compared to the traditional PLC control platform reduced 60.53%.

Conclusion

Through control system performance test, the system uses CPLD parallel features achieving multi-RS485 bus control at the same time and DSP chip is introduced in a certain extent, improve the system's real-time and data processing ability. The new reference scheme are provided for the development of motor and the multi motor synchronous control, which has strong practicability and popularization value.

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