Analytical Model of Channel Electric Field Profile in FinFET

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Abstract—**A simple analytical model for the lateral channel electric field profile in the velocity saturation region of the FinFET with undoped body is proposed and developed by solving the Poisson Equation in the velocity saturation region with a simplified boundary condition. The model has been verified with two-dimensional numerical device simulators and good agreement is obtained. Using the model, the impact of geometrical parameters including silicon film thickness, gate oxide thickness, and the terminal biases on the maximum lateral channel electric field in the FinFET can be predicted.**

Keywords-double-gate MOSFET; FinFET; channel electrical field; velocity saturation

I. INTRODUCTION

As the scaling of bulk CMOS is approaching to the limit, double-gate (DG) MOSFETs such as FinFET have been considered to be the ultimately scalable CMOS technology due to their better immunity to short channel effect (SCE), better current drive and almost ideal subthreshold slope [1,2]. However, the hot-carrier effects such as the channel hot-carrier injection, impact ionization induced breakdown and device degradation pose other limits on the scaling of FinFET. To study the hot-carrier effects and their consequence, a channel electric field model, especially the maximum electric field at the end of the channel should be developed.

In this paper, an analytical channel electric field model based on a pseudo two-dimensional analysis in the velocity saturation region of FinFET with undoped body is proposed and developed. The model is extensively verified by a two-dimensional numerical device simulator MEDICI. The impact of scaling of physical parameters including silicon film thickness, gate oxide thickness, and channel length on the maximum channel electrical field is evaluated.

II. MODEL

For the device operating in saturation regime, the channel of the Symmetric DG MOSFET, e.g. FinFET can be divided into gradual channel approximation (GCA) region and velocity saturation region (VSR). A schematic cross-section of the VSR of a FinFET with undoped body is shown in Figure 1. “Boundary 1” in the figure indicates the located in the channel where the velocity of carriers just saturates.

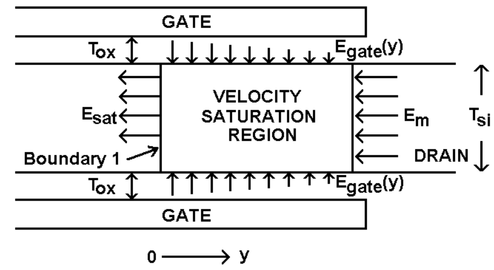

FIGURE I. A CROSS-SECTION OF THE SYMMETRICAL DG MOSFET WITH UNDOPED BODY. THE RECTANGULAR BOX ENCLOSED BY THE SOLID LINE IS THE VELOCITY SATURATION REGION WHERE GAUSS’S LAW IS APPLIED

The model is developed based on the pseudo two-dimensional approach proposed by Elmansy [3] and Ko [4]. Gauss’s law is applied to the VSR (Figure 1)

$$\varepsilon_{si}\int_{-\frac{Tsi}{2}}^{\frac{Tsi}{2}} E_{sat}\cdot dx-\varepsilon_{si}\int_{-\frac{Tsi}{2}}^{\frac{Tsi}{2}}\frac{\partial V}{\partial y}\cdot dx-2\varepsilon_{gate}\int_{0}^{y}E_{gate}(k)\cdot dk=-q\int_{-\frac{Tsi}{2}}^{\frac{Tsi}{2}}\int_{0}^{y}Q(x,k)\cdot dkdx \tag{1}$$

where ε_{si} and ε_{gate} are the dielectric coefficient of silicon and gate insulator, respectively. T_{si} is the silicon film thickness, and Q is the mobile charge concentration per unit volume. To account for the non-uniformity distribution of the lateral electric field, it is assumed that the ratio of average lateral electric field to the surface lateral electric field in the VSR is independent of position y and is equal to the value at boundary 1 [3]

$$\int_{-\frac{Tsi}{2}}^{\frac{Tsi}{2}}\frac{\partial V}{\partial y}\cdot dx=A\cdot Tsi\cdot\frac{dV_s}{dy} \tag{2}$$

where V_s is the surface potential. The value of A at boundary 1 can be calculated using the vertical potential profile proposed by Yuan [5]

$$V(x)=-\frac{2kT}{q}\ln\left[\cos\left(B\cdot x\right)\right]+V_o \tag{3}$$

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where V_o is the potential at the center of the silicon film and $B = \sqrt{\frac{q^2 n_i}{2\varepsilon_{si} kT}} \cdot e^{\frac{qV_o}{2kT}}$. For simplicity, the potential profile is approximated by a parabolic function with a fitting parameter K

$$V(x) \approx K \cdot x^2 + V_o \tag{4}$$

Since the parameter K will be eliminated in the calculation of A, the exact value of K is not shown in the following calculations. The value of A is calculated by substituting (4) into (2)

$$A = \frac{1}{3} + \frac{2}{3} \cdot \frac{\partial V_o}{\partial V_s} \tag{5}$$

The partial derivative in (5) is calculated using equation (3)

$$A = \frac{1}{3} + \frac{2}{3\left(1 + \frac{B \cdot T_{si}}{2} \cdot \tan\left(\frac{B \cdot T_{si}}{2}\right)\right)} \tag{6}$$

Substituting (2) into (1) and differentiating both sides with respect to y, we get

$$\varepsilon_{si} \cdot A \cdot T_{si} \cdot \frac{d^2 V_s}{dy^2} = q \int_{-\frac{Tsi}{2}}^{\frac{Tsi}{2}} Q(x,y)dx - 2\varepsilon_{gate} \cdot E_{gate}(y) \tag{7}$$

The integrated mobile charge term in (7) can be replaced by the gate electric field at boundary 1 with the assumption that GCA still holds at that location. Equation (7) becomes

$$\varepsilon_{si} \cdot A \cdot T_{si} \cdot \frac{d^2 V_s}{dy^2} = 2\varepsilon_{gate} \cdot \left[E_{gate}(0) - E_{gate}(y)\right] \tag{8}$$

Since the gate electric field can be expressed as $E_{gate}(y) = \frac{V_g - V_{FB} - V_s(y)}{T_{gate}}$, where V_g and V_{FB} is the gate and flat band voltage, respectively. T_{gate} is the gate insulator thickness. Equation (8) is rewritten to

$$\frac{d^2 V_s}{dy^2} = \frac{\left[V_s(y) - V_s(0)\right]}{\lambda^2} \tag{9a}$$

and

$$\lambda = \sqrt{\frac{A \cdot \varepsilon_{si}}{2\varepsilon_{gate}}} \cdot \left(T_{si}\right)^{\frac{1}{m}} \cdot \left(T_{gate}\right)^{\frac{1}{n}} \tag{9b}$$

with $m = n = 2$. Using the boundary condition $V_s(0) = V_{dsat}$ and $\frac{dV_s(y)}{dy}|_{y=0} = E_{sat}$ at boundary 1, the solution of equation (9a) is given by

$$E(y) = E_{sat} \cdot \cosh(\frac{y}{\lambda}) \tag{10}$$

and

$$V(y) = V_{dsat} + \lambda \cdot E_{sat} \cdot \sinh(\frac{y}{\lambda}) \tag{11}$$

It can be shown that the maximum lateral electric field (E_m) at the end of the channel is

$$E_m = \sqrt{\frac{\left(V_d - V_{dsat}\right)^2}{\lambda^2} + E_{sat}^2} \tag{12}$$

where V_d is voltage at the end of the channel.

III. Results and Discussion

A 0.05µm SDG N-MOSFET with mid-gap work function gate-electrode and silicon dioxide gate insulator is used as a vehicle for the following simulations to evaluate the model. Extensive numerical simulations with MEDICI show that the parameter m in equation (9b) should be linearly from 2.03 to 1.97 as the T_{si} increasing from 5nm to 20nm. Figure 2 compares the results calculated from the model with the results obtained from MEDICI for the SDG device with T_{ox} =2nm, T_{si} = 10nm and E_{sat} = 3.5x10^4 V/cm [6]. Good agreement, is obtained between the model and the 2D simulation result especially near the peak E-field region where hot carrier effects is the most serious.

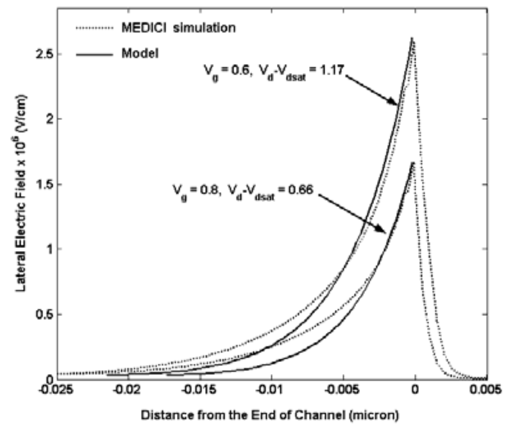

FIGURE II. COMPARISON OF THE RESULTS CALCULATED FROM THE MODEL WITH THE RESULTS OBTAINED FROM THE SIMULATIONS FOR THE SDG DEVICE WITH T_{ox} = 2nm, T_{si} = 10nm AND E_{sat} = 3.5x10^4 V/cm.

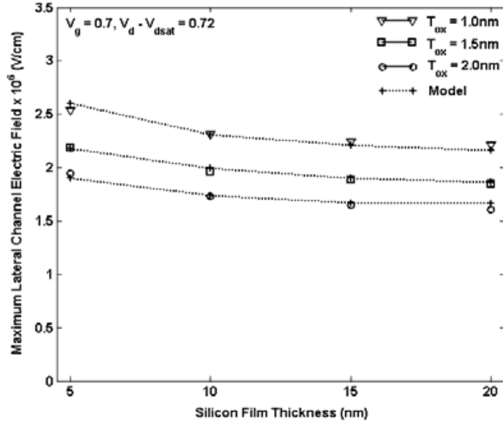

FIGURE III. THE PLOT OF THE MAXIMUM LATERAL CHANNEL ELECTRIC FIELD (E_m) AGAINST THE SILICON FILM THICKNESS (T_{si}) AS A FUNCTION OF THE GATE OXIDE THICKNESS.

Figure 3 shows the maximum lateral channel electric field (E_m) versus the silicon film thickness (T_{si}) with different gate oxide thickness (T_{ox}) under the same biasing condition. The results from the model, again, show good agreement with the simulation results. As predicted by the model, the maximum electrical field increases with the reduction of T_{si} and T_{ox}. The impact of geometry scaling is included through λ which does not have an obvious scaling trend. However, there is a maximum value of λ which can be obtained by replacing the parameter A with its minimum value, giving $\lambda_{\max} = \sqrt{\frac{\varepsilon_{si}}{6\varepsilon_{gate}}} \cdot (T_{si})^{\frac{1}{m}} \cdot (T_{gate})^{\frac{1}{n}}$. This λ_{max} is an important parameter to calculate the maximum E_m and evaluate the worst-case hot-carrier effects for a given SDG structure and biasing condition.

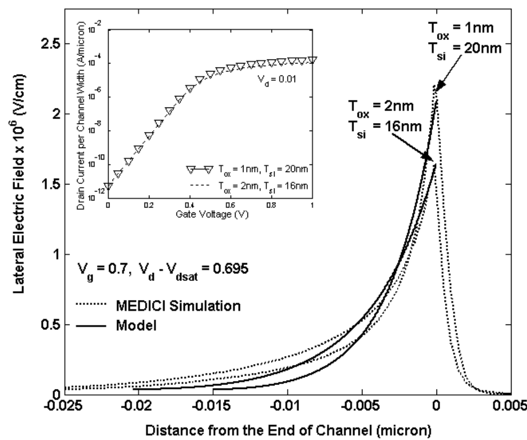

FIGURE IV. COMPARISONS OF THE LATERAL ELECTRIC FIELD FOR TWO SDG DEVICES WITH SAME OFF-STAGE CURRENT AND THRESHOLD VOLTAGE, BUT DIFFERENT PHYSICAL PARAMETERS SUCH AS T_{ox} = 1nm, T_{si} = 20nm and T_{ox} = 2nm, T_{si} = 16nm.

Figure 4 shows the lateral electric field for two SDG devices with same off-stage current and threshold voltage, but different T_{ox} and T_{si} with value shown in the figure. The I_d - V_g characteristic of those SDG devices are shown as an insert in Figure 4. The results show that, those SDG devices have similar DC characteristic, but different E_m. Although scaling either the T_{si} or the T_{ox} can give us the same performance (e.g. off-stage current), the hot-carrier effects is more seriously affected by the scaling of T_{ox}. It also suggests that our proposed model can be used to study how different scaling approaches affect the hot-carrier effects.

IV. Conclusion

We have presented a simple analytical model for the lateral channel electric field in the velocity saturation region of the FinFET with undoped body. This model compares well with the results obtained from the numerical two-dimensional simulator MEDICI. We also introduce an important parameter λ_{max} to characteristic the worst-case hot-carrier effects in a given FinFET structure and biasing condition. This model is simple and helpful to understand how the scaling of FinFET device affecting the hot-carrier effects.

Acknowledgments

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