

Design of Low Phase Noise and Low Stray Frequency Source Based on FPGA+HMC833

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Abstract—Microwave resonator sensor has been applied to various fields of measurement. A frequency source with low phase noise, low stray, low power consumption, small step is the key to measurement of microwave resonator sensor. In order to adapt the requirements of the measurement, this paper selects and uses HMC833 phase locked loop (PLL) chip to design frequency source, and uses FPGA to control PLL chip, designs a reliable frequency source through taking full advantage of FPGA and low phase noise and low stray of HMC833. At last of this paper, test results show that the frequency source can meet each requirement.

Keywords-FPGA; HMC833; low phase noise and low stray; phase locked loop

I. INTRODUCTION

Microwave resonator sensor as a passive wireless sensor can be used in a variety of fields well^[1]. To do this, we need a wide operating frequency band, high precision and high stability frequency source to stimulate the cavity of the sensor. FPGA device using the standardized structure, is small volume, high integration, low power consumption and high speed. FPGA can be infinitely repeated programming, and the application is very broad. The criteria to judge the frequency source contains frequency width and frequency resolution, tuning time, phase noise and spurious suppression. A good frequency source is as much as possible to make low phase noise and spurious^[2].

This article using FPGA as the main control chip, and using the a chip-- HMC833LP6GE, produced by company Hittite, as phase locked loop frequency signal chip, develops a set of frequency source that can be used in microwave resonator sensors.

II. GENERAL STRUCTURE OF SYSTEM

The function of the frequency source designed by this article is generating $5000\pm 1000\text{MHz}$ signal. The frequency source is mainly composed of four groups: the generating part of radio frequency signal, the control of data reading and writing, the reference input signal and the loop filter. The system overall structure block diagram is shown as Fig. 1. The communication between FPGA to HMC833 and the control of the register in the HMC833 are key point. Whether the performance of the loop filter is good or bad will directly relate to the noise of the VCO, the locking time of loop filter and the phase noise of the crystal and discriminator.

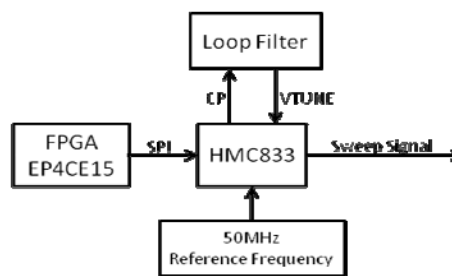


FIGURE I. OVERALL STRUCTURE BLOCK DIAGRAM OF THE SYSTEM

III. THE DESIGN OF THE HARDWARE

A. The Selection of Reference Frequency Signal

The design selection of the reference frequency signal is the Hittite HMC1031MS8E integer N points frequency PLL clock generator, it's characteristics are as follows: low power consumption, high frequency phase detection, phase detection instructions and power down mode.

B. The Design of the Loop Filter

The loop filter circuit diagram is shown as Fig. 2. Its bandwidth needs some consideration when designing the filter and this article design the parameters of the loop filter with the aid of Hittite PLL Design^[3,4].

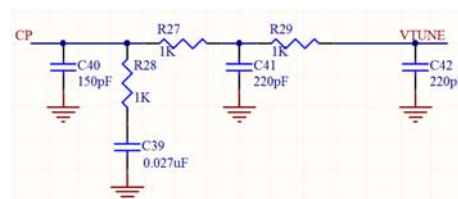


FIGURE II. THE LOOP FILTER CIRCUIT DIAGRAM

C. HMC833 Peripheral Circuit Design

The peripheral circuit is shown as Fig. 3. Reference signal pass through the pin XREFP into the chip, after R divider, and then sent to the phase discriminator. The output of the discriminator pass through the charge pump, and then sent to the loop filter through the pin CP. After filtering and then from the pin VTUNE to control the VCO, VCO signal through a programmable frequency divider to control, finally, the RF - N output.

External control signal through the SEN, SDI, SCK pin written into the chip internal registers in the form of bus; Locking pin Ln-SD0 not only can configuration monitor output, also can output the internal register values; CEN is chip enable port which is high level efficient; BIAS, as the BIAS circuit decoupling, need a series capacitor grounding; The rest of the port are the power input and idle pin.

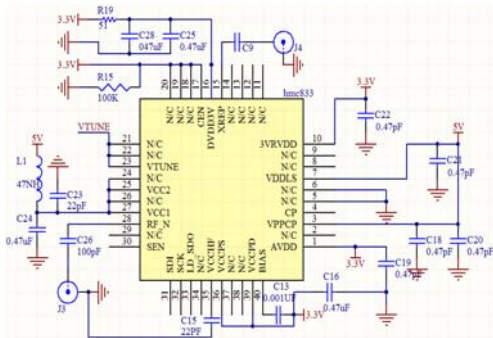


FIGURE III. THE PERIPHERAL CIRCUIT OF HMC833

IV. THE DESIGN OF SOFTWARE

The chip used in this design is a chip produced by Altera company--EP4CE15F17C8, and the control program written uses Verilog language, its control flow chart as shown in Fig. 4. First, the system confirms the start frequency, end frequency and the step according to the user input through the button. Second, the system initials the HMC833 registers according to the input. Third, the system runs as the command set before. During the sweeping, the system changes the frequency through updating the register of the HMC833 Reg 03h and Reg 04h^[5].

The HMC833 has 18 HMC833 internal PLL and 7 VCO registers. This design to register initialization settings and sequence is as follows (the register didn't mention here are change according to the official manual to default values, Reg 03h and Reg 04h are based on user input) :

- (1) Reg 00h= 0x000000;
- (2) Reg 00h= 0x0a7975;
- (3) Reg 06h= 0x000002;
- (4) Reg 09h= 0x547FFF;
- (5) Reg 0ah= 0x002046;
- (6) Reg 0bh= 0x07C021;
- (7) Reg 10h= 0x0000b2;
- (8) Reg 11h= 0x080002;
- (9) Reg 12h= 0x000003;
- (10) Reg 05h= 0x000188;
- (11) Reg 05h= 0x00a090;
- (12) Reg 05h= 0x002898;
- (13) Reg 05h= 0x002018;
- (14) Reg 05h= 0x001628;

(15) Reg 05h= 0x0060a0;

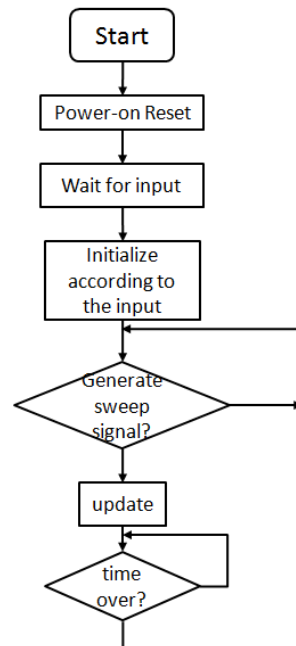


FIGURE IV. FPGA CONTROL FLOW CHART

Form written writing data is based on the SPI bus and sequence diagram as shown in Fig. 5.

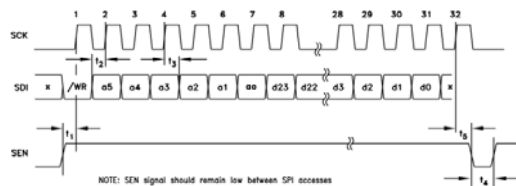


FIGURE V. HMC833 SPI WRITE OPERATION SEQUENCE DIAGRAM

A write operation includes the following steps:

- (1) The Master (host) places 24-bit data, d23:d0, MSB first, on SDI on the first 24 falling edges of SCLK.
- (2) the slave (HMC833LP6GE) shifts in data on SDI on the first 24 rising edges of SCLK
- (3) Master places 5-bit register address to be written to, r4:r0, MSB first, on the next 5 falling edges of SCLK(25-29)
- (4) Slave shifts the register bits on the next 5 rising edges of SCLK (25-29).
- (5) Master places 3-bit chip address, a2:a0, MSB first, on the next 3 falling edges of SCLK (30-32). Hittite reserves chip address a2:a0 = 000 for all RF PLL with Integrated VCOs.
- (6) Slave shifts the chip address bits on the next 3 rising edges of SCLK (30-32).
- (7) Master asserts SEN after the 32nd rising edge of SCLK.
- (8) Slave registers the SDI data on the rising edge of SEN

The design software module as RTL view of SPI is shown in Fig. 6.

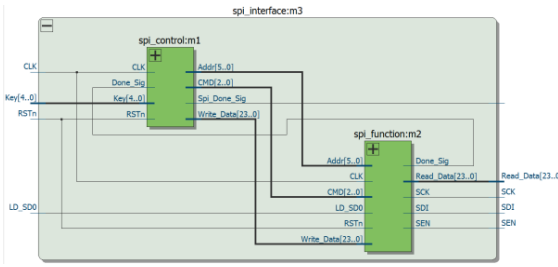


FIGURE VI. SPI DESIGN RTL VIEW

The FPGA pin configuration of SPI is shown as Fig. 7

OUT	SPI_Out[3]	Output	PIN_L1
OUT	SPI_Out[2]	Output	PIN_N1
OUT	SPI_Out[1]	Output	PIN_L2
OUT	SPI_Out[0]	Output	PIN_P1

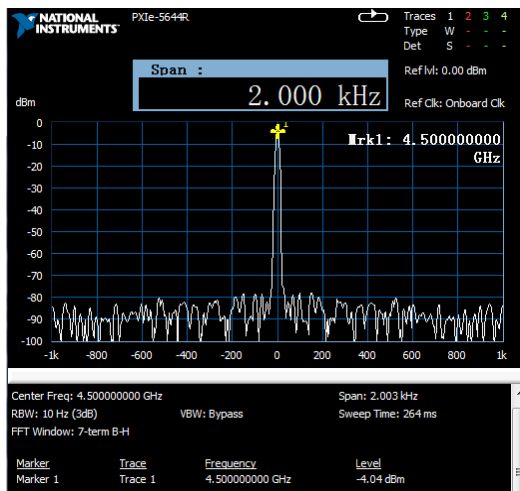
FIGURE VII. SPI PIN CONFIGURATION

V. THE TEST RESULTS AND ANALYSIS

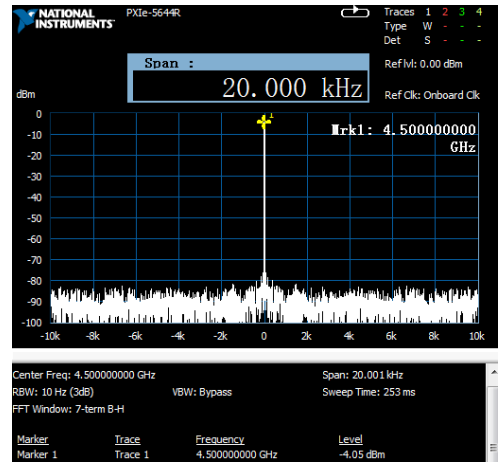
This article uses the device of NI PXIe-5644 vector signal analyzer to detect phase noise and analyze the stray of the frequency source. Test results are shown as Fig. 8.

Figure 8 (a), (b), (c) are the measurement of frequency source phase noise and spurious under the situation that the source continuously send frequency at 4.5GHz. Test results as follows: when the frequency at 1 kHz, the phase noise reached 121.3dBc/Hz, and the result almost the same when the frequency change to 10 kHz, and the stray inhibition reached to -81dBc; Figure 8 (d) is the measurement of frequency source in 4~5 GHz frequency sweep signal process, you can see each frequency point error can limit within 1 kHz.

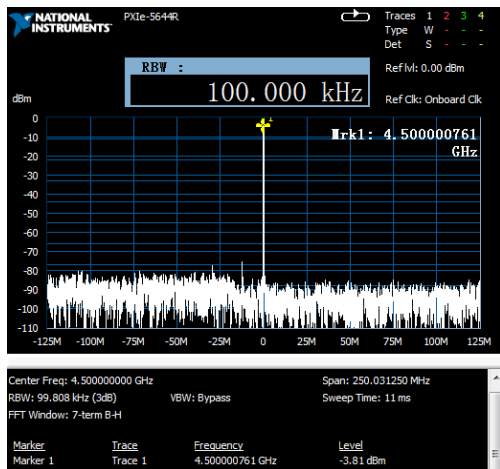
Visibly, the frequency source designed by this article has high stray inhibition degree, fully meet the requirements of system for signal source.



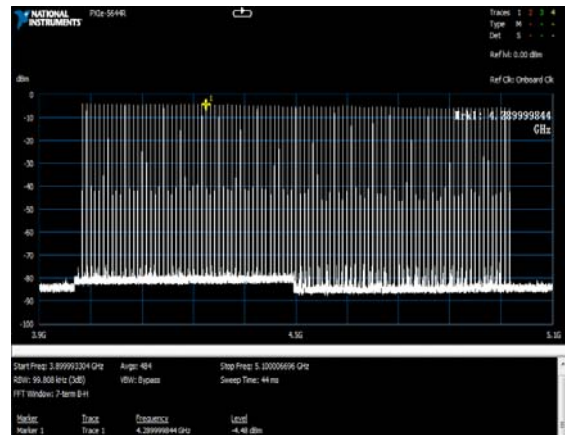
(a)



(b)



(c)



(d)

FIGURE VIII. THE TEST RESULTS: (a) 1KHZ PHASE NOISE; (b) 10KHZ PHASE NOISE; (c) STRAY; (d) 4~5GHZ SWEEP PROCESS CONCLUSION

This paper introduces the use of the Hittite HMC833 start-up phase lock loop and Altera company launched EP4CE15F17C8 chip, designed a low phase noise, low spurious frequency source. By FPGA to register HMC833 reasonable configuration, got the good frequency sweep signal

output, have great significance in engineering. Test results show that this design can suppress frequency source phase noise and spurious degree is very good, can be used for other incentives of microwave resonator sensor signal source.

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