The Grid Inverter of Negative Sequence Compensation Rapid Phase-Lock Control Strategy

Jin Xu[1], Lin Li[2] and Sanqin Zhao[2]
[1]College of Engineering, Nanjing Agricultural University
[2]The Key Laboratory in the Aspect of Intelligent Agricultural Equipment, Jiangsu Province

***Abstract*—Aiming at the shortage of traditional phase-locked method in the three-phase unbalanced conditions of power grid, this paper proposed a novel software phase-locked loop control strategy. This paper introduces in detail the working principle and designing method of the digital PLL by comparative experiment. The experimental results demonstrated that the new method is feasible and robust. In conclusion, the new control algorithm can quickly and accurately detect the correct phase voltage.**

Keywords-rapid phase lock; voltage; unbalanced grid voltages; grid voltage dips; grid inverter; negative sequence compensation

I. INTRODUCTION

Currently, the digital phase test of power grid has been widely applied. Various methods were proposed in diverse fields [1] such as hardware detection of Zero-crossing of power grid [2]. However the method is susceptible to interference and not suitable for a fault grid phase. Software phase lock methods usually adopt the low-pass filter, notch filter and band-pass filter to obtain angle information of the grid to detect positive and negative sequence components by converting the Three-phase voltage coordinates to Two-phase coordinate system [3-5]. How-ever, the use of the filter will lead to a big lag. Moreover open-loop method will usually cause some steady-state error.

In order to solve the problems stated above. Karimi-Ghartemani et al. [6] created an open-loop detection method based on extended Kalman filter. However, the implementation of the method is difficult thereby preventing the practical application. The design of Closed-loop detection method was described by Chung [7] which was known as PLL technology. Its main drawback is the frequency fluctuations. The appearance of the negative sequence component in grid= will result in twice the grid frequency fluctuations in the dq coordinate system, affecting the lock-in effect. Rodriguez et al proposed a dual synchronous coordinate system to eliminate the influence of the negative sequence component [4]. However, this method will cause a lot of delays in system through using a low-pass filter. Timbus described a method capable of decoupling dual synchronous coordinate system [8], but which still requires the use of multiple low-pass filter to obtain the positive sequence negative sequence voltage amplitude. Karimi-Ghartemani [9] introduced a method which can eliminate double fluctuations of the grid frequency by using the repetitive controller. But, only simple simulation waveforms are given without taking the realization into consideration.

Aiming at the shortcomings of the above methods, a new type of Three-phase digital PLL of Negative sequence compensation rapid phase-lock was proposed in this paper. First, the effect of unbalanced grid fault on traditional three phase locked-loop was analyzed. Second, the working principle and design of the new PPL were described. Finally, the experiments were carried out in the experimental platform with TI's TMS320F28335 as the main chip.

II. MATHEMATICAL MODEL OF RAPID PHASE-LOCKED LOOP CONTROL STRATEGY

A. Three Phase Digital PLL Principle

Figure 1 shows the topology structure of negative sequence compensation rapid lock control system of three-phase unbalanced grid-connected inverter. Where PV is a group of string battery panels i_a , i_b , i_c is the grid-side three-phase current; U_d is the voltage of battery panels.

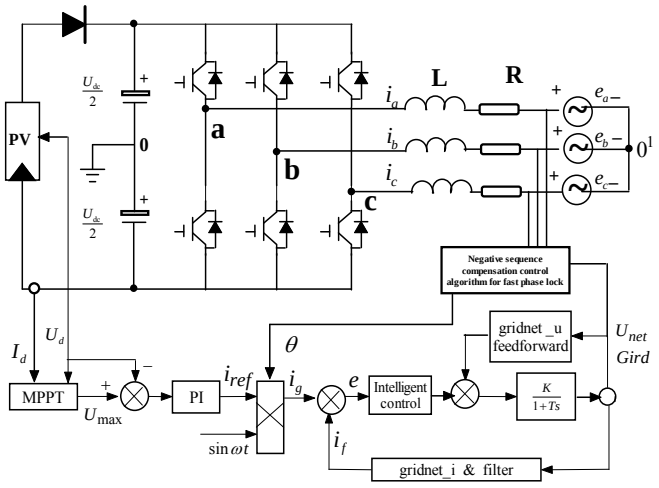

FIGURE I. TOPOLOGY STRUCTURE OF THREE-PHASE UNBALANCED GRID INVERTER

Figure 2 is a structure diagram of software phase lock of the traditional dq coordinate conversion. To guarantee lock-in successfully in the symmetrical voltage grid, We used the 3/2 (abc /) coordinate conversion and) coordinate conversion to adjust the AC voltage component to 0 through the PI regulator. [11-13].

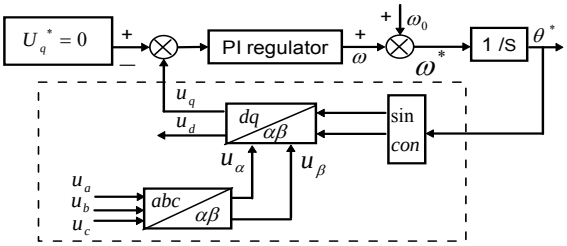

FIGURE II. THE STRUCTURE DIAGRAM OF SOFTWARE PLL IN TRADITIONAL DQ TRANSFORM

Figure 3 is an improved structure diagram of the software rapid phase lock in three-phase unbalance. It is an improvement of traditional dq transforms phase-lock by adding negative sequence compensation component, using a simple sine wave to achieve the purpose of compensating the negative sequence components of the grid.

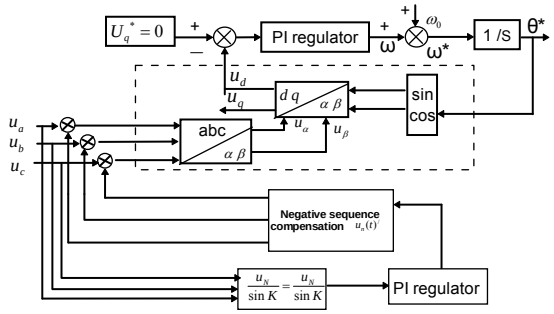

FIGURE III. THE STRUCTURE DIAGRAM OF RAPID PHASE-LOCK CONTROL

III. UNBALANCE CONTROL STRATEGY OF NEGATIVE SEQUENCE COMPENSATION

The in the formula (1) is the fundamental voltage of grid. According to the method of symmetrical components, the component can be divided into positive, negative and zero sequence symmetrical components.

$$u(t) = u_p(t) + u_n(t) + u_z(t) \tag{1}$$

where $u_p(t)$, $u_n(t)$, $u_z(t)$ are positive sequence component, negative sequence component, and zero-sequence component respectively, which can be expressed as

$$\begin{cases} u_p(t) = \begin{bmatrix} u_{pa} \\ u_{pb} \\ u_{pc} \end{bmatrix} = \begin{bmatrix} U_{pm}\sin(\omega_p t+\varphi) \\ U_{pm}\sin(\omega_p t+\varphi-2\pi/3) \\ U_{pm}\sin(\omega_p t+\varphi+2\pi/3) \end{bmatrix} \\ u_n(t) = \begin{bmatrix} u_{na} \\ u_{nb} \\ u_{nc} \end{bmatrix} = \begin{bmatrix} U_{nm}\sin(\omega_{np} t+\varphi) \\ U_{nm}\sin(\omega_n t+\varphi+2\pi/3) \\ U_{nm}\sin(\omega_{np} t+\varphi-2\pi/3) \end{bmatrix} \\ u_z(t) = \begin{bmatrix} u_{za} \\ u_{zb} \\ u_{zc} \end{bmatrix} = \begin{bmatrix} U_{zm}\sin(\omega_n t+\varphi) \\ U_{zm}\sin(\omega_p t+\varphi-2\pi/3) \\ U_{zm}\sin(\omega_p t+\varphi+2\pi/3) \end{bmatrix} \end{cases} \tag{2}$$

$$u_n'(t) = \begin{bmatrix} u_{na}' \\ u_{nb}' \\ u_{nc}' \end{bmatrix} = \begin{bmatrix} U_{nm}'\sin(\omega_{np} t+\varphi) \\ U_{nm}'\sin(\omega_n t+\varphi+2\pi/3) \\ U_{nm}'\sin(\omega_{np} t+\varphi-2\pi/3) \end{bmatrix} \tag{3}$$

where $u_n'(t)$ is the compensation of three-phase unbalance.

Since the three-phase grid connected inverter adopted phase 3- wire system, there is no zero-sequence current component. Zero-sequence voltage has no influence on the inverter grid phase lock as it will change into 0 after coordinate transformation. Therefore, only the positive sequence component and negative sequence component will be discussed [13].

The sampled three-phase voltage plus negative sequence compensation is calculated as below

$$u(t) = u_p(t) + u_n(t) - u_n(t) \tag{4}$$

$$u(t) = \begin{bmatrix} U_{pm}\sin(\omega_p t+\varphi) \\ U_{pm}\sin(\omega_p t+\varphi-2\pi/3) \\ U_{pm}\sin(\omega_p t+\varphi+2\pi/3) \end{bmatrix} + \begin{bmatrix} U_{nm}\sin(\omega_{np} t+\varphi) \\ U_{nm}\sin(\omega_n t+\varphi+2\pi/3) \\ U_{nm}\sin(\omega_{np} t+\varphi-2\pi/3) \end{bmatrix} - \begin{bmatrix} U_{nm}'\sin(\omega_{np} t+\varphi) \\ U_{nm}'\sin(\omega_n t+\varphi+2\pi/3) \\ U_{nm}'\sin(\omega_{np} t+\varphi-2\pi/3) \end{bmatrix} \tag{5}$$

where U_{nm} is the peak of Negative sequence voltage, φ is the phase angle of the negative sequence, ω_{np} is the angular frequency of the second harmonic

$$u_n(t)-u_n'(t) = \begin{bmatrix} U_{nm}\sin(\omega_{np} t+\varphi) \\ U_{nm}\sin(\omega_n t+\varphi+2\pi/3) \\ U_{nm}\sin(\omega_{np} t+\varphi-\pi/3) \end{bmatrix} - \begin{bmatrix} U_{nm}'\sin(\omega_{np} t+\varphi) \\ U_{nm}'\sin(\omega_{np} t+\varphi+2\pi/3) \\ U_{nm}'\sin(\omega_{np} t+\varphi-2\pi/3) \end{bmatrix} = \begin{bmatrix} (U_{nm}-U_{nm}')\sin(\omega_{np} t+\varphi) \\ (U_{nm}-U_{nm}')\sin(\omega_{np} t+\varphi+2\pi/3) \\ (U_{nm}-U_{nm}')\sin(\omega_{np} t+\varphi-2\pi/3) \end{bmatrix} \tag{6}$$

A. Control Strategy

Problem is then transformed into the equivalent one how to compensate the negative sequence component of the actual grid voltage. Namely, how to adjust the amplitude (U_{nm}') of the negative sequence compensation amount to make the formula (7) establish.

$$\frac{\sin N}{u_N} = \frac{\sin K}{u_K} \tag{7}$$

where u_N and u_K are AC power grid voltage instantaneous value at point N and point K, sinN, sinK are the grid's AC sine value of point N and point K (point N and point K is the Random sampling point of grid voltage).

For balanced three-phase power grid, the following formula will be established.

$$e_K = u_? \times sinN - u \times sinK \quad (8)$$

$$\delta = u_n(t) - u_n'(t) \quad (9)$$

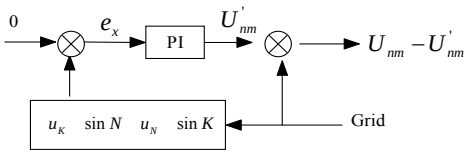

FIGURE IV. THE STRUCTURE DIAGRAM OF RAPID PHASE-LOCKED CONTROL STRATEGY

IV. Experimental Results

In order to further validate the proposed control method, the experimental platform with TI's TMS320F28335 as the main chip is constructed. The parameter of this 100 kW grid inverter is: WPAP330150 AC grid power supply and 150 kW DC analog power, maximum DC power and AC power are 150kw. It can simulate a variety of unbalanced voltages such as 1kv DC open circuit voltage.

In this experimental system, a variety of different sources of the three-phase unbalanced grid were simulated through AC grid simulation. In addition, the comparative experiments with rapid phase lock control strategy were conducted.

Figure 5 shows the waveforms of input grid voltage from three-phase equilibrium state to that with one phase unbalanced. B phase changes from normal to the state with 40% of asymmetry in the decreasing process, while the A phase and C phase remain unchanged.

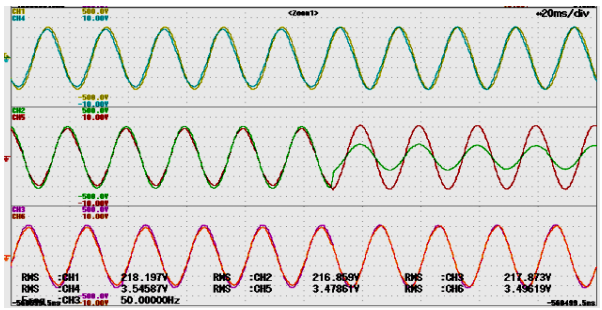

FIGURE V. VOLTAGE AND CURRENT WAVEFORMS OF B PHASE 40% OF IMBALANCE

As can be seen from Figure 5, voltage and current of both A-phase and C-phase keep unchanged, while B-phase voltage has a 40% of unbalance. In this case the three-phase currents and power are constant, and the current is smooth and is not distorted (Since no suitable testing instruments are available, the phase locked situation is validated by using the phase of the grid current here). The results demonstrated that the control algorithm can overcome the effects of negative sequence component through quickly following the phase of grid during the process of grid voltage changing into unbalance.

Figure 6 shows the voltage and current waveforms under the condition of B-phase 60% asymmetry. Figure 7 is the waveform under the condition of 40% asymmetry of two phases. Figure 8 is the waveform under the conditions of 20% asymmetry of two phases. Judging from the experimental waveforms, the phase lock can be successfully implemented by negative compensation algorithm.

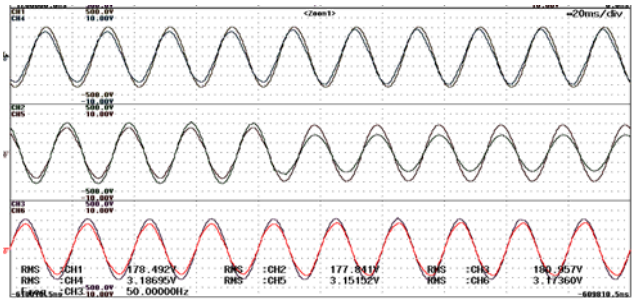

FIGURE VI. VOLTAGE AND CURRENT WAVEFORMS UNDER THE CONDITION OF B PHASE 60% IMBALANCE

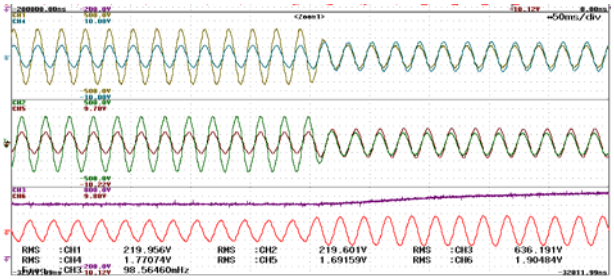

FIGURE VII. VOLTAGE AND CURRENT WAVEFORMS UNDER THE CONDITION OF A AND B PHASE 40% IMBALANCE

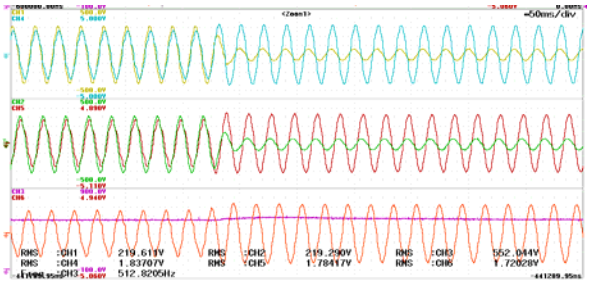

FIGURE VIII. VOLTAGE AND CURRENT WAVEFORMS UNDER THE CONDITION OF A AND B PHASE 20% IMBALANCE

In order to validate whether the control strategies can quickly and accurately lock phase under diverse power situations, the power grid was adjusted to 50% of the rated load. Under this condition, shown as Figure 9 and Figure 10, the grid voltage changes was also changed to the 30% of the original rated voltage.

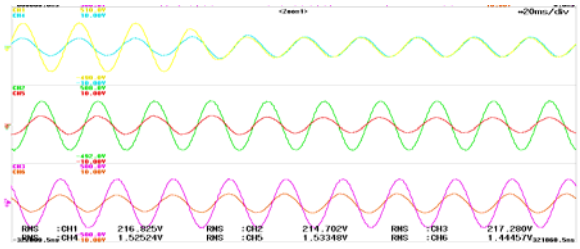

FIGURE IX. THERE-PHASE-UNBALANCE PHASE- CLOCKED WAVEFORM UNDER DIFFERENT POWERS

In the instant of grid voltage fluctuation, the conventional phase lock-in technique control strategy is powerless to deal with the instantaneous power fluctuations thereby leading to the

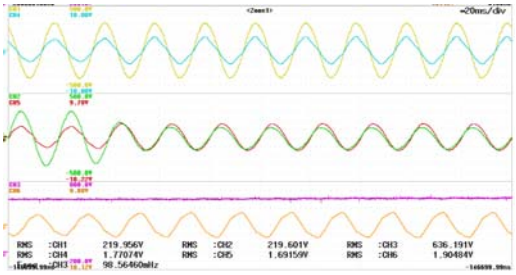

FIGURE X. AC VOLTAGE AND CURRENT, DC VOLTAGE WAVEFORMS UNDER THE CONDITION OF GRID 30% IMBALANCE

Corresponding fluctuation in DC side output voltage. However, a smooth and stable DC voltage can be realized by the negative sequence compensation rapid phase-locked control strategy. When the grid is unbalanced, , the AC side voltage of PV inverter Down to 20% of the rated condition causes a sudden decreases of the active power output. However, with the adoption of this control strategy, PV inverter can keep grid connected operation. The AC side output cur-rent recovered to the rated current value after a short adjustment process during the fault period. Although the current during the fault slightly increases, it can be successfully limited within the range of 1.1 times of rated current after a short adjustment process. The control strategy basically limits the current increase and protects the inverter power electronic devices. The reduction of power output leaded to the in-crease of the cumulative energy in DC side of the inverter capacitor, thereby subsequently resulting in the DC voltage increase due to the capacitor charging effects. While, the DC side current reduced during fault period.

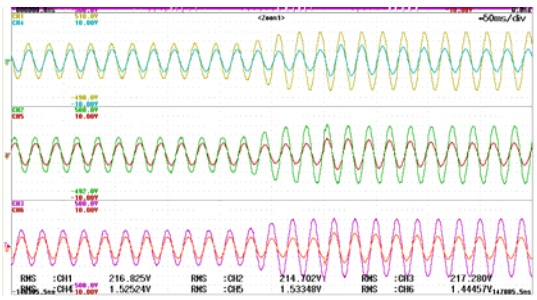

FIGURE XI. THE WAVEFORM UNDER THE CONDITION OF THE RECOVERY OF THE UNBALANCED THREE PHASE VOLTAGE TO NORMAL

Figure 11 shows the waveforms of unbalanced grid voltage recovering from unbalance to normal. The results show that the proposed algorithm can effectively track the input signal at the moment of voltage changing.

V. CONCLUSIONS

Aiming at the imprecision of phase locking of three-phase photovoltaic grid inverter during the power grid voltage unbalance, this work proposed a closed-loop control method of negative sequence compensation to subtly and quickly realize the imbalance of grid phase locking by simple sub-traction algorithm. This method replaces the traditional zero-capture hardware phase lock circuit, achieving a phase lock on software. Furthermore it may be applied to fast and accurately phase lock, frequency lock, obtain current grid information and achieve the requirement of grid connection in a variety of conditions, , such as Grid frequency mutations, Grid with harmonics, Grid voltage amplitude low and so on.

The reliability of the algorithm was verified under various power imbalance conditions

- Experiments of three-phase power phase lock in which one phase voltage is unbalanced.
- Experiments of three-phase power phase lock in which two phases' voltage are unbalanced.
- Experiments of three-phase power phase lock recovery from unbalance to balance;
- DC bus voltage fluctuation test in unbalanced three-phase grid;
- Phase lock experiments of Three-phase grid from unbalance to balance.

Experimental results demonstrated that the rapid phase lock control strategy presented above is feasible which is easy to be implemented and stable under a variety of imbalance conditions. The accuracy and reliability of the proposed control strategy have been validated by experiments.

REFERENCES

[1] Svensson, J. "Synchronisation methods for grid-connected voltage source converters". Generation, Transmission and Distribution, IEE Proceedings, IEE Proceedings, IET. Vol. 148, No. 3, pp. 229-235, 2001.

[2] Song, H.-S. and K. Nam, "Instantaneous phase-angle estimation algorithm under unbalanced voltage-sag conditions," IEE Proceedings-Generation, Transmission and Distribution. Vol. 147, No. 6, pp. 409-415, 2000.

[3] Wu, X., et al., "Virtual admittance control scheme of three-phase PWM rectifier under un-balanced input voltage condition," Electric Power Automation Equipment, Vol. 30, No. 3, pp. 35-39, 2010.

[4] Rodriguez, P., L. Sainz, and J. Bergas. "Synchronous double reference frame PLL applied to a unified power quality conditioner," Harmonics and Quality of Power, 2002. 10th International Conference on. pp. 614-619, 2002.

[5] Roiu, D., et al., "New stationary frame control scheme for three-phase PWM rectifiers under unbalanced voltage dips conditions," Industry Applications, IEEE Transactions on, Vol.46, No. 1, pp. 268-277, 2010.

[6] Karimi-Ghartemani, M. and M.R. Iravani, "A method for synchronization of power electronic converters in polluted and variable-

frequency environments," Power Systems, IEEE Transactions on, Vol. 19, No. 3, pp. 1263-1270, 2004.

[7] Chung, S.-K., "A phase tracking system for three phase utility interface inverters," Power Electronics, IEEE Transactions on, Vol. 15, No. 3, pp. 431-438, 2000.

[8] Timbus, A.V., et al. PLL algorithm for power generation systems robust to grid voltage faults. in Power Electronics Specialists Conference, 2006. PESC'06. 37th IEEE. 2006. IEEE.

[9] Karimi-Ghartemani, M., "A novel three-phase magnitude-phase-locked loop system," Circuits and Systems I: Regular Papers, IEEE Transactions on, Vol. 53, No. 3, pp. 1792-1802, 2006.

[10] Zhang, X., et al., "Study of internal model control based three-phase PWM rectifier under unbalanced input voltage condition," PROCEEDINGS-CHINESE SOCIETY OF ELECTRICAL ENGINEERING, Vol. 25, No. 13, pp. 51, 2005.

[11] Chen, M.-k., et al., "Application of fan-in vector method in detection of harmonics and reactive current," PROCEEDINGS-CHINESE SOCIETY OF ELECTRICAL ENGINEERING, Vol. 28, No. 7, pp. 110, 2008.

[12] Zhou, J., L. Chen, and P. Zhou, "Contrastive research on improved synchronous reference frame method and detecting method based on sequence extractor of positive and negative fun-damental wave for detecting current," Journal of Central South University: Science and Technology, Vol. 39, No. 4, pp. 816-823, 2008.

[13] Etxeberria-Otadui, I., et al., "New optimized PWM VSC control structures and strategies under unbalanced voltage transients." Industrial Electronics, IEEE Transactions on, Vol. 54, No. 5, pp. 2902-2914, 2007.