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The Integrity of 28nm HK/MG nMOSFETs Probed with Drain Bias Stress

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***Abstract*—Adopting coupling drain bias stresses to probe the device integrity achieved the good consequences in the study of device leakage, interface state, and oxide trap causing some degradation effect in the tested devices and observed the GCIP effect at the higher drain stress conditions.**

Keywords-impact ionization; leakage; DIBL; MOSFET; drain; trap; GCIP effect; high-k

I. INTRODUCTION

Due to the few researches investigating the degradation of nano-node n-channel metal-oxide-semiconductor field-effect transistor (nMOSFET) and the leakage under the drain bias, but the leakage current related to the OFF-current is one of important factor for MOSFET performance, therefore, the main study in this article focused on this trend and probed the interface state, oxide integrity, leakage and device performance in increasing cycle sweep under this kind of drain bias for nMOSFET.

In this work, we adopted the 28nm high-k/metal-gate (HK/MG) process fabricating the tested devices from UMC to do the related extraction and analysis. In this research, there were two test conditions: one was to set bias of drain terminal from 0 to 3V which the sweep time was from one to ten and the degradation phenomena of the tested MOSFET in threshold voltage (V_T) and drive current (I_{DS}) were recorded. The other was to set bias of drain terminal from 0 to 5V and the characteristics of device leakage could be sensed. The former test condition was analyzed after the experiment which we could possibly expose the increase of interface state and oxide trap of tested devices with increasing stress cycle times in short-channel device and these extracted results would illustrate the induced degradation of device leakage in the end, but after about five-times stress, the degradation level would close to saturation; the degradation degree through the increase of stress times became not obvious if the chosen channel length increased 2-4 times compared with the tested short-channel device. In the other test condition, the slope of leakage was different from that after drain bias to 3 V in short channel due to the serious drain-induced barrier-lowering (DIBL) effect accelerating the inversion charges to hit the drain site. The electron-hole pairs (EHPs) will be generated by impact ionization. Finally, this phenomenon will induce avalanche effect; the main mechanism is band-to-band tunneling (BTBT) effect dominant in long-channel tested device due to the slope of source leakage (I_S) at the tested MOSFET wasn't distinctly different, but when the depletion region at the drain zone will be raised by the increase of drain bias, the depletion region at the source terminal will be possibly bridged both sides. This phenomenon will cause the punch-through effect. As the drain bias is still increased, the gate-current-induced punch-through (GCIP) effect will be possibly observed, depending on the tested channel length.

II. TESTED CONDITIONS

A. Verification of Original Tested Devices

To obtain a normal tested device, the basic characteristics such as source/drain current (I_{DS}), threshold voltage, trans-conductance (G_m) and subthreshold swing (SS) must be extracted to satisfy the specification. Then, the tested sample can be treated as a qualified sample if all of the extracted performance is passed. One of the tested devices with the schematic cross-sectional profile is demonstrated in Fig. 1.

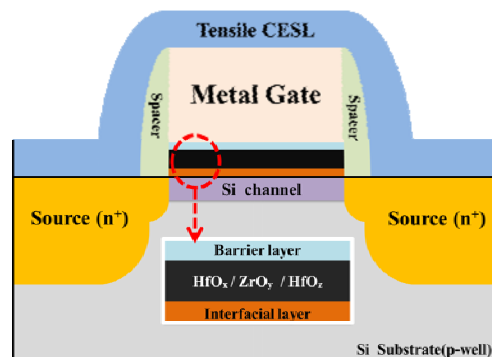

FIGURE I. SCHEMATIC CROSS-SECTION OF AN NMOSFET WITH HK/MG STRUCTURE

The drive current can illustrate the switching speed of a MOSFET. The G_m and SS variables are able to demonstrate the channel mobility (μ) and the interface quality between channel surface and interfacial layer in gate dielectric, respectively. The original test conditions are listed in Table 1.

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TABLE I. ORIGINAL TESTED DEVICES WITH SCREENING CONDITIONS AS CHANNEL LENGTH W= 1.0 µm

Vcc (V)	0.8
Channel length (µm)	0.03, 0.04, 0.07, 0.15, 0.5, 1
Temperature (°C)	25
V_T extraction	Constant current
V_{GS}-V_T (V)	Vcc

The extraction methods for obtaining the threshold voltage usually have two species: maximum G_m extraction [1] and constant current extraction [2].

B. Choosing the Suitable Stress Conditions in Drain and Gate Sides

In the formal experiment, we chose the feasible test devices and conditions after the screening procedures. The stress conditions and tested devices are represented in Table 2. In principle, the gate, source and bulk electrodes for tested MOSFETs are grounded.

TABLE II. STRESS CONDITIONS WITH ONE CYCLE AND 10 CYCLES

	Parameters	
Dielectric	$HfO_2/ZrO_2/HfO_2$ ($HfZrO_2$)	
V_{CC} (V)	0.8	
Stress mode	Cycle	Breakdown
Dimension(µm)	W=1, L=0.03, 0.04,0.07, 0.15	W=1, L=0.03, 0.04, 0.07, 0.15, 0.5, 1
Stress voltage (V)	V_D=0~3, V_B=V_S=V_G=0	V_D=0~5, V_B=V_S=V_G=0
Sweep cycle	10	1
Temperature(℃)	25	

III. TEST RESULTS AND DISCUSSION

Before the stress conditions, the original characteristics of the tested devices are extracted to be some references justifying the deviation level after the stress experiments. For a drive current of an nMOSFET (I_{DS}), it can be represented as

$$I_{DS} = \frac{W}{2L}\mu_n \cdot C_{ox} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS}) \qquad (1)$$

where C_{OX}: gate capacitance with unit area and : channel-length modulation factor. To increase the C_{OX}, the high-k gate dielectric such as HfO_2 (k~ 25) [3] is applied into the advanced nano-node semiconductor process.

Figure 2 shows the original drive current with solid circle and the stressed drive current with open circle as well as the various channel-length devices. The I_D-V_D characteristics are extracted with the same original extraction method after ten cycle stresses. According to the test results, we see that the worst degradation of the drain current at the same vertical field, V_{GS}-V_T, is the shortest channel device. With the increase of the tested channel length, the degradation effect is gradually not obvious due to the decrease of the channel field.

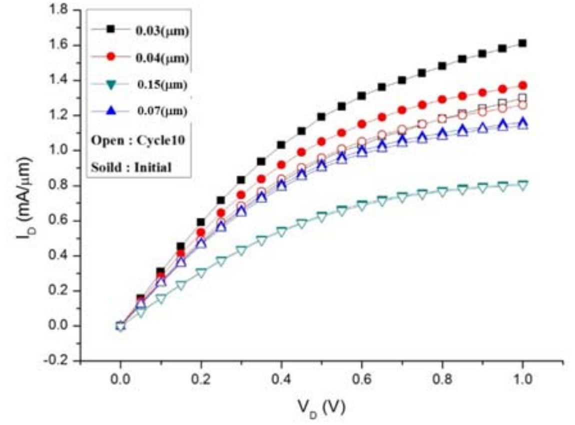

FIGURE II. I_D-V_D PERFORMANCE FOR NMOSFETS WITH DIFFERENT CYCLE STRESSES AND TESTED CHANNEL-LENGTH DEVICES

As we discuss the device performance, the parameter, subthreshold swing (SS), should be considered due to the index of interface quality and the off-leakage such as gate-induced drain leakage (GIDL) effect [1] as well as the switching quality for this device. The SS can be defined as

$$SS = \left(\frac{d\log(I_{DS})}{dV_G}\right)^{-1} = 2.3\frac{kT}{q}\left(1 + \frac{C_d + C_{it}}{C_{OX}}\right) \qquad (2)$$

where k: Boltzmann constant, T: absolute temperature, C_d: depletion capacitance in channel surface, and C_{it}: equivalent interface-state capacitance. The unit of SS is V/decade.

After the test, we observe that the shortest channel device after a ten cycle stress showed the increase of the SS value and declined the degradation mechanism to the punch-through phenomenon, as shown in Fig. 3.

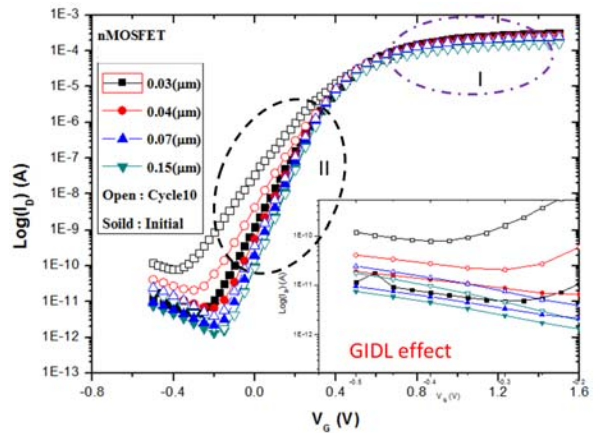

FIGURE III. CHARACTERISTICS OF SUBTHRESHOLD SWING FOR COUPLE TESTED DEVICES BEFORE AND AFTER DRAIN STRESS. THE GIDL EFFECT IS LOCATED AT THE SUBSET

In zone I of Fig.2, the dominant mechanism of drain current is attributed to the diffusion, but the drift domination in zone II. In the subset, the tested shortest channel device after a ten cycle stress represented the worst GIDL effect, which meant that the shortest device could provide the highest current, but the degradation risk increased due to the increase of horizontal field in channel.

While the stress action is followed, the device degradation is simultaneously turned on. Following the V_T equation [2] grounding the substrate bias, it can be expressed as

$$V_T = \phi_{ms} - \frac{Q_f}{C_{OX}} - \frac{Q_d}{C_{OX}} + 2\phi_b \tag{3}$$

where $_{ms}$: work function difference between gate electrode and channel bulk, Q_f: fixed charge including the oxide trap and the interface state, Q_d: depletion charge in channel surface and $_b$= $(E_i$-$E_F)/q$ =$(\ln(N_a/n_i))kT/q$ which E_i: intrinsic Fermi level, E_F: Fermi level, q: unit charge, N_a: substrate concentration, and n_i: intrinsic concentration of silicon wafer. When the V_T change is observed, the fixed charge is basically increased in the number of interface state (N_{it}), oxide trap (N_{ot}), or both, as shown in Fig. 4.

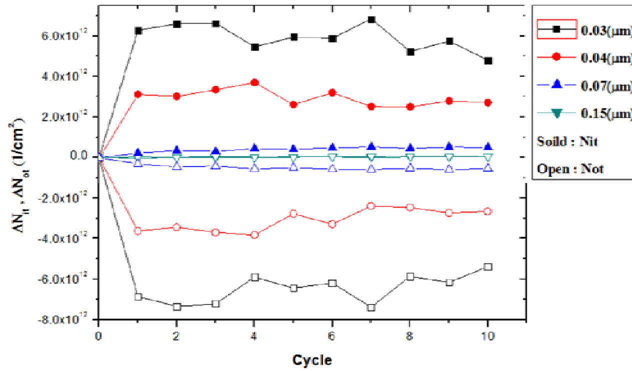

FIGURE IV. THE VARIATION OF INTERFACE STATE NUMBER AND OXIDE TRAP NUMBER WITH CYCLE STRESSES AND CHANNEL LENGTHS

According to (2), the difference of C_{it} = q D_{it} before and after stress can be extracted as [1]

$$N_{it} = \int D_{it} \cdot dE \approx D_{it} \cdot E_{it} \tag{4}$$

$$\Delta N_{it} = \frac{\Delta SS \cdot C_{OX} \cdot E_{it}}{2.3 \cdot kT} \tag{5}$$

where E_{it} is the energy range in which the active interface states distributed. Here, E_{it} = q $_b$ is based on the average channel doping concentration.

The fixed charges in device are generally classified as N_{it} and N_{ot} for the advanced semiconductor process, excluding the mobile ion contribution. The total change charge number N_{total} is equal to N_{it}+ N_{ot}.

$$\Delta N_{total} = \frac{\Delta V_T \cdot C_{OX}}{q} \tag{6}$$

In Fig. 4, the generation amount of N_{it} and N_{ot} at the shortest channel device is the largest and the electron type at N_{it} characteristic is trapped. On the contrary, the hole carriers trapped contribute to the N_{ot}. With the increase of the tested channel lengths, the degradation is obscure.

The trans-conductance G_m is also a good index to expose the interface quality located at the channel surface, comparing before and after stress, as shown in Fig. 5. For a drain current operating at the linear region, it can be expressed as (7) and the G_m at the fixed V_{DS} can be given as (8)

$$I_{DS,lin} = \frac{W}{L} \cdot \mu \cdot C_{OX} \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) \cdot V_{DS} \tag{7}$$

$$G_m = \frac{\partial I_{DS}}{\partial V_{GS}} |_{V_{DS}=0.05V} = \frac{W}{L} \cdot \mu \cdot C_{OX} \tag{8}$$

In (8), the possible variable is the channel mobility. Thus, the G_m change can linearly represent the channel mobility change, as shown in Fig. 5. We also observe that the G_m change after drain bias stress is increased as the tested channel length is decreased, which means the surface scattering effect is increased, causing the drain current decreased.

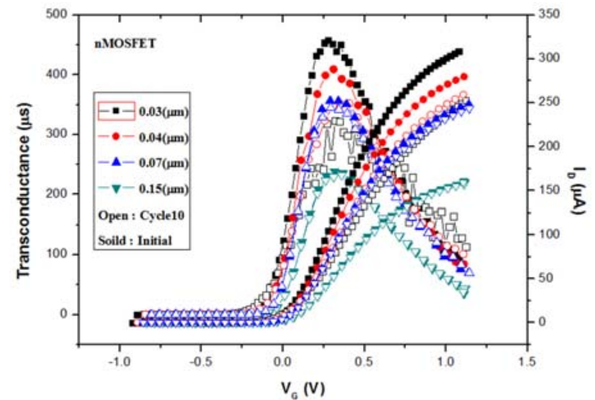

FIGURE V. CHARACTERISTICS OF Gm AND LINEAR $I_{DS,lin}$ VS. V_G FOR DIFFERENT TESTED DEVICES AND STRESS CYCLES

Considering a whole leakage in an nMOSFET, there are, at least, five species: I_1: direct tunneling leakage, I_2: subthreshold leakage, I_3: GIDL current, I_4: punch-through leakage, and I_5: BTBT current, as shown in Fig. 6. Investigating the OFF-state current of a tested device, W/L=1/0.03 (μm/μm) due to the distinct degradation after the drain bias stress, the initial leakage distribution is exhibited in Fig. 7.

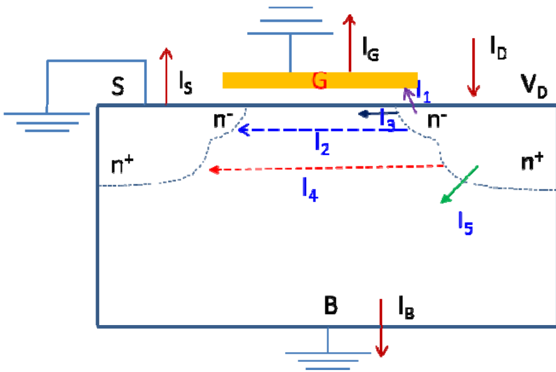

FIGURE VI. THE WHOLE LEAKAGE DISTRIBUTION IN AN NMOSFET

It also can be classified as three leakage mechanisms: subthreshold (Sub.) leakage, DIBL induced leakage, and impact ionization. The leakage percentage is listed at Table 3. The leakage from drain to source is the highest. The gate leakage is the smallest. After ten cycle stress, the IS and IG are increased more, as shown in Fig. 8.

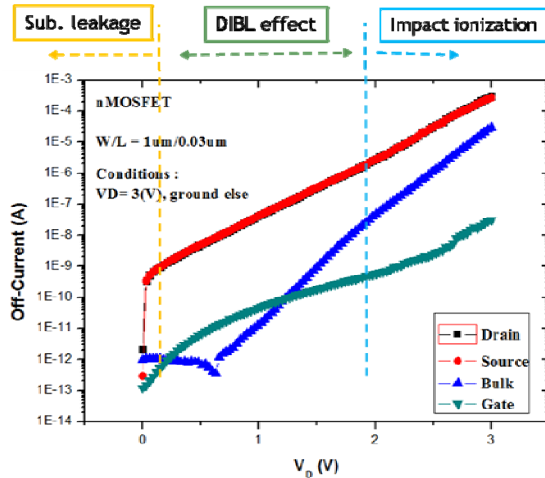

FIGURE VII. INITIAL LEAKAGE DISTRIBUTION FOR AN NMOSFET

TABLE III. LEAKAGE DISTRIBUTION OF A W/L= 1/0.03 (μm/μm) DEVICE BEFORE STRESS

1/0.03 (μm)	The definition : $I_D = I_S + I_B + I_G$			
$V_D = 3(V)$	I_D	I_S	I_B	I_G
leakage current	3.03E-04	2.73E-04	2.98E-05	3.10E-08
Percentage(%)	100	90.14	9.83	0.01

However, as the drain bias is increased to 5V, some special phenomenon at long-channel devices such as L ≥ 0.15 m is observed, as shown in Fig. 9. The I_S curve demonstrates a turning point at $V_D \approx 3.4$V, called V_{GCIP}. This effect [4] is due to the increase of drain voltage inducing more electron carriers coming from the gate electrode and generating the EHPs by the drain zone. More hole carriers move to the source terminal with the diffusion mechanism. However, this effect is not overt at the short channel devices.

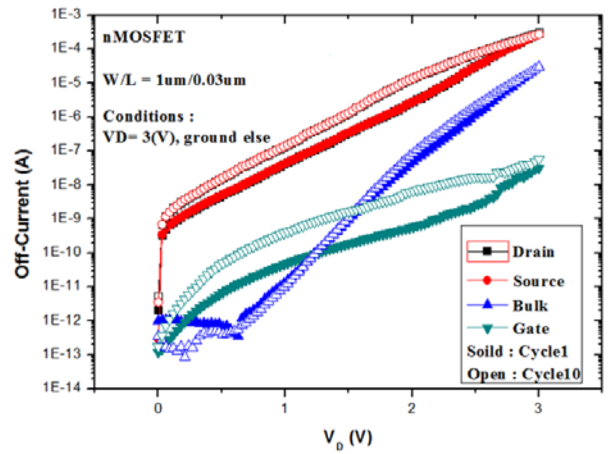

FIGURE VIII. THE LEAKAGE DISTRIBUTION FOR THE SHORTEST CHANNEL DEVICE AFTER DRAIN STRESS WITH VD=3V

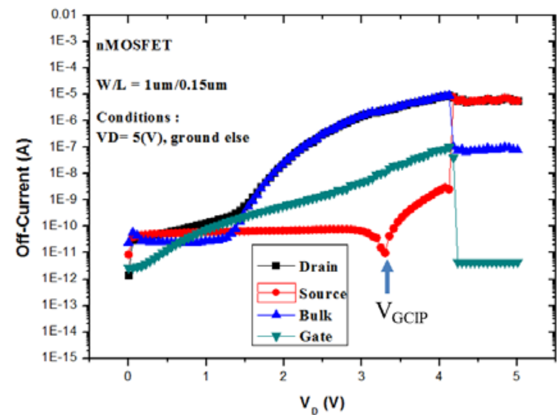

FIGURE IX. LEAKAGE DISTRIBUTION FOR A LONG CHANNEL DEVICE AT VD=5V

IV. CONCLUSION

Using a drain bias stress, the integrity of nano-node MOSFETs can be justified. With the more cycles of drain bias stress, the device endurance in electrical field consideration can be classified. In the long-channel condition, the source leakage has the reverse phenomenon with the high drain voltage and this phenomenon has the behavior attributing to the hot electron tunneling from drain to source region. Furthermore, the EHP induced by the impact ionization is possibly the main reason for the electron diffusion that the source leakage raises up after its current direction is reversely changed. Finally, the punch-through effect induced by depletion region touching called a GCIP mechanism was observed.

In the shorter-channel devices, the DIBL is probably the main domination that the effect induces the inversion charge from source to drain region which increases and hits the drain side. Therefore, the DIBL has leaded the EHPs by impact ionization for high field condition in the drain side. If the inversion charge inducing the EHPs has the behavior of recombination, the source leakage will be increased seriously.

When the EHPs are more and more increased, they will induce to the avalanche effect. The DIBL effect has the serious influence when the channel length is shorter than 0.15µm in this test.

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