

High-speed Image Acquisition and Network Transmission System Based on FPGA

Hao Wang, Zhi Weng* and Xiaochun Li

College of Electronic Information Engineering, Inner Mongolia University, Hohhot 010021, China

*Corresponding author

Abstract—Through the study of the Camera Link interface protocol, the Ethernet protocol, and the VGA display sequence, the writer designs a high-speed image acquisition and network transmission system based on FPGA (Field-Programmable Gate Array) CMOS (Complementary Metal Oxide Semiconductor) and details the system structure as well. The system uses FPGA to drive CMOS image sensor for collecting the image data, and DDR3 module for data caching. Through controlling the Ethernet interface chip by the FPGA master control chip, the systems can achieve high-speed data transmission and transmit the image data to the upper computer for display or to the VGA (Video Graphics Array) for display on the screen. The system achieves high-speed image data acquisition, storage, remote transmission and display.

Keywords—FPGA; Ethernet; Image acquisition; Master computer; Labview

I. INTRODUCTION

Along with the continuous development of the digital image technology and large integrated circuit technology, the embedded image processing system especially the miniaturization of it is gaining more and more attention in the application of image processing and transmission, such as application to military target tracking, the terrain matching, and war-field information acquisition, etc[1]. As for videophone conference on communication, combination and recognition of faces in criminal investigation and remote monitoring, etc., there are other issues should be concerned. Due to a large amount of image data and the calculation is complex, the requirements of the high speed, there is a need for CMOS image mining system to be designed based on FPGA. The system, in which large amounts of data are adopts FPGA parallel processing method, makes the acquisition speed increased significantly, as to meet the requirements of real-time image processing, high integration of FPGA and CMOS, real-time processing of large amount of data, and the trend that Ethernet network of long-distance transmission becoming the main transmission method in image acquisition processing [2]. High-speed image acquisition and network transmission system are discussed in this system.

II. SYSTEM CONCEPTUAL DESIGN

The hardware of image data acquisition and network transmission system hardware mainly includes two parts: the FPGA core system with data acquisition and transmission part. Core system includes FPGA master control chip, Altera

specific configuration chip EPCS (Erasable Programmable Configurable Serial), data cache chip SDRAM (Synchronous Dynamic Random Access Memory) and other main parts. Channel acquisition and transmission part mainly include Camera Link channel connector MDR26, deserializer conversion chip DS90CR288AMTD, differential signal conversion chip DS90LV019MTC, VGA interface, network protocol conversion chip e1111 RCJ - 88 and other major parts. Block diagram of overall system is shown in figure I.

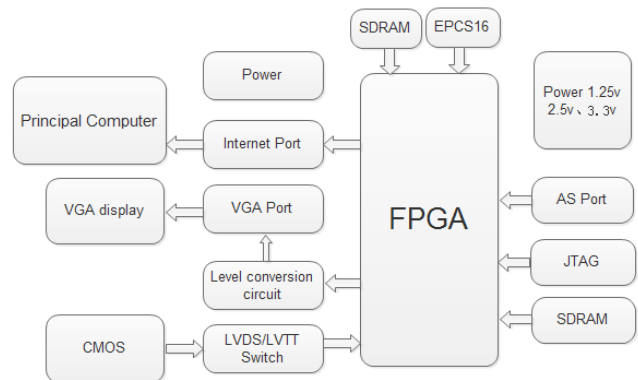


FIGURE I. BLOCK DIAGRAM OF OVERALL SYSTEM

The core system mainly contains a core processor EP4CE6F17C8, which is FPGA from the CYCLONE IV series of Altera Company. The FPGA has rich on-chip resources (6272 LE in total); maximum storage space upon 276480 bit; there are 392 multipliers; maximum available I/O for 179 users. Its powerful processing capabilities and plenty of resources can completely meet the requirements of design, and carry on the four MT46V64M16 caches, increasing the storage space of the system, and the cache is mainly used to collect the real-time image data for storage, which can meet the real-time image acquisition, processing, transmission and lay a solid foundation for data transmission and display.

In data acquisition and transmission part, the data acquisition channel is composed of two pieces of signal conversion chip DS90CR288AMTD, because the Camera Link technology adoption is an LVDS (Low Voltage Differential Signal) for transmission, on the receiving end there is need to convert the differential signal to signals compatible with the processor of CMOS or TTL. DS90CR288AMTD converts 4 LVDS signals to 28 road parallel data signals which are output to the FPGA while there is a clock signal as a synchronous

clock being output into the FPGA. The channel section contains the VGA display interface and the NIC driver module for image acquisition and transmission task. Image data collected is transmitted to the PC through the network interface, and the PC completes image stitching, developing and other processing.

III. SYSTEM MODULE DESIGN

This design adopts common design method of FPGA: the top-down design method for system design. The design content is divided into the following several main parts: image acquisition design, data storage design, VGA display control network implementation, communication module design and channel calibration module design.

A. Image Acquisition Design

The sampling part needs image acquisition as 32-bit parallel image data, image acquisition module's clock is provided by a single-ended signal from the output of the camera clock and converted by DS90CR288 (deteriorated conversion chip solution). Because the camera clock and memory module clock's frequency are different, there is a problem of the Cross Clock Domain, and to solve this problem generally uses FIFO and dual port RAM solution [3]. This design uses the PLL double frequency to output 500 MHz clock camera clock for sampling, with sampling clock as the synchronous clock of acquisition module, data collected goes through dual port RAM for temporary storage and then is archived to SRAM, which needs an interface control module for the process of collection to storage. The function block diagram is shown in figure II.

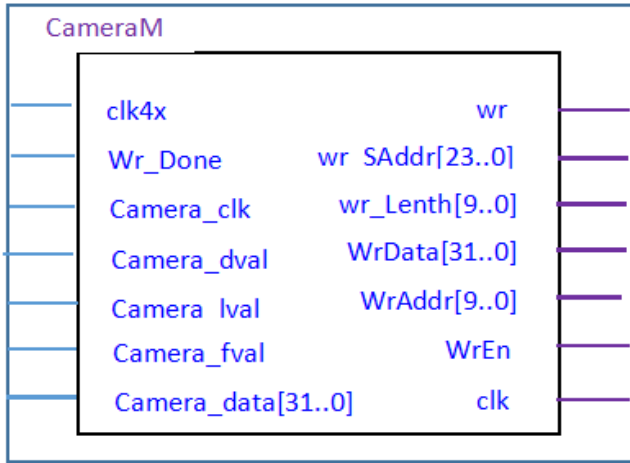


FIGURE II. FUNCTION BLOCK DIAGRAM OF IMAGE ACQUISITION

Clk4x input signal is for the input clock, it is composed of a signal, which comes from a doubling of the system clock frequency by the FPGA internal PLL. And then with clk4x for sensitive signals, samples the camera clock sampling and the sampling clock is assigned to CLK outputs, as the clock domain memory write clock, which helps the follow-up function module be in the same phase of the clock source. Camera_data [31.. 0] is camera output image data after being deserializing; Camera_clk cameras is the clock signal, when Camera_dval is detected to be effective, write an effective

signal to RAM, and send written address out, and when Camera_fval effects, the Wr_SAddr increases, in charge of SDRAM address, WrdData [31.. 0] is written to the transition SRAM cache at first, and then stored in SDRAM. WrAddr [9..0] is write address of memory in transition memory, and when Camera_data is effective, send the transition register SRAM's write command WrEn. After storing a row of data, SDRAM becomes write effective, RAM becomes read-effective.

B. Data Storage Design

Data collected by the Camera Link interface needs caching, then to be carried on the post-processing. The System contains the DDR SDRAM, every two pieces in a group. One group of cache memory is used for caching display data; another set of memory is used for caching display data. Ping-pong operation is applied to collect data cache [4], its principle is shown in figure III. Data storage selection circuit is responsible for data writing to A or B s and issuing written instructions, realizing the rotation of memory writing of A and B; Data output selection unit is responsible for the data reading from A or B memory and sends read instructions, realizing the rotation of memory reading operation of A and B memory. The read/write operations of memories transmit the image data in real-time to the data processing module for next processes.

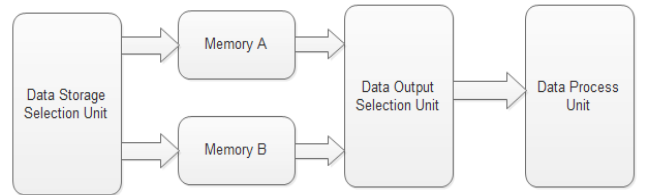


FIGURE III. SCHEMATIC DIAGRAM OF PING-PONG OPERATION

Because this design needs to store a large amount of image data, it uses the peripheral memory SDRAM. By operating each group of SDRAMs' different cache in turns to read and write, it completes the Ping-pong operation. At some time point, the write operations on memory group A takes place at the same time when read operation is taken on memory group B; the next moment is to take read operation on memory group A, and write operation on memory group B write operations, and circulation of read/write operation on two pieces of memory achieves the goal of real-time.

C. VGA Display Control Design

In order to achieve the real-time display of collected images, the data to be displayed needs to be done through FIFO data cache[5]. In the data effective zone of displaying, the VGA controller sends commands to read the FIFO data, to meet the requirements of VGA display's time sequence. In summary, the principle diagram of the function is shown in figure IV.

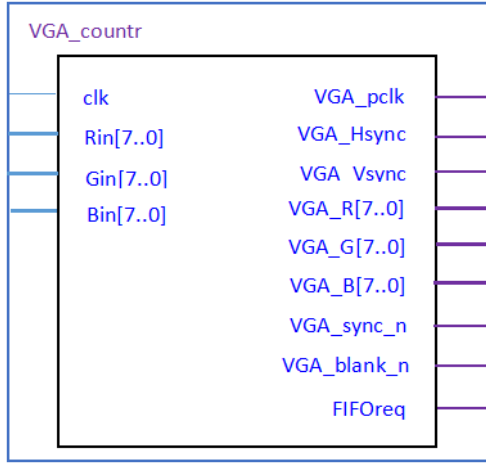


FIGURE IV. THE PRINCIPLE DIAGRAM OF THE FUNCTION FOR VGA DISPLAY CONTROL

In this paper, the design of the resolution of the image display is 1280 x1024 @ 60 MHZ, with a clock frequency of 108 MHZ. According to the selected display resolution and within the application, the counter counts to determine the field synchronization and line synchronization control signals. When making counting of Line scan, 112 line sync pulses are counted at first, then going through 248 pulses' data efficient frontiers, and when the counter become 360, it comes into rows of data activation and VGA_Hsync was pulled into the valid state. After finished scanning one line, the counter reset and field counter adds 1, at the same time when the counter counts to the 41, it comes into field activation segment, and VGA_Vsyn was pulled into the valid state. The data between line activation segment and field activated segment is in the valid data area, then it will be displayed on a screen, meanwhile, effective data area FIFO is pulled int high and send memory a data request command.

D. Network Communication Module Design

Collected image data needs to be uploaded to the terminal control system for the post data processing and image reduction, reproduce, and so on. This requires communication between acquisition system and PC. The design use Ethernet interface to transmit image data, which does encapsulation to the image data to be sent as form suited for network transmission, and then send packed data to the PC via Ethernet interface. This paper uses the UDP transport protocol to transmit [6]. The underlying data's encapsulation is shown in figure V.

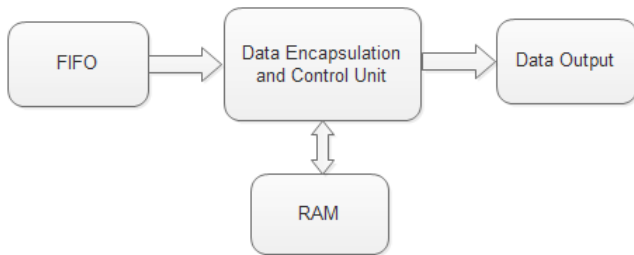


FIGURE V. FLOW DIAGRAM OF DATA ENCAPSULATION

In the data transmission part, for the real-time of the transmission and the continuity of data flow, the first step is to send the data into the FIFO, then the encapsulate control unit controls data reading from the FIFO. When data transmission going on, the control unit sends read instructions to FIFO to read data from a FIFO for checksum calculation, and at the same time send a write instruction to RAM, to store data read into RAM at the assigned space in due order. When the length of data read equals the length of data sent, the FIFO read instruction will be set as invalid, the checksum calculation will be finished as well, and then the checksum is inserted into the appropriate location in the header of the data packet, which is the specified address in RAM. When a packet of data is completely packed, the control unit will send a write instruction to RAM to upload the packed data.

E. Upper Computer Software Design

Upper PC is the part for the interaction between the whole system and user, in this system it is mainly responsible for the control of the beginning and the end of the image data acquisition, to restore the data collected into image and display, and can provide observation of channel correction before FPGA collecting data at the same time Correction. Upper computer software is programmed by Labview[7, 8]. Graphical interface of Labview is shown in figure VI.

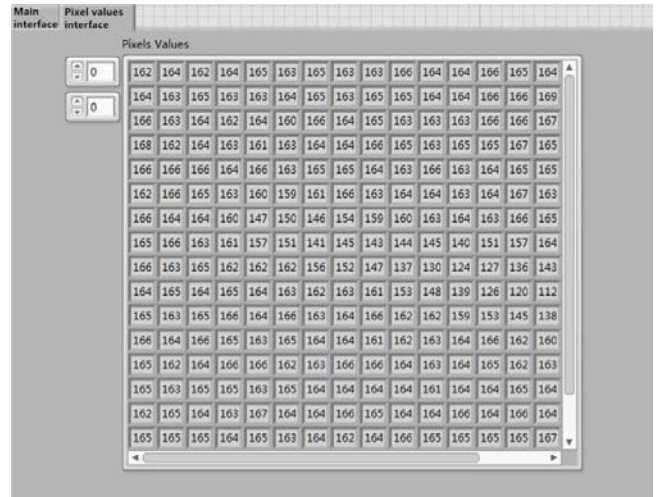


FIGURE VI. GRAPHICAL INTERFACE OF LABVIEW

IV. THE RESULT OF SYSTEM TEST

After the system modules design and debugging, next step is to connect every system parts, including the image sensor, data acquisition card, and PC. Then after the system is tested OK, the system gets access to electricity. Using the JTAG downloader can download the program to the PROM configuration chip in FPGA. After downloading all programs, the system resets, and waits for the system for automatic configuration, including CMOS image sensor initialization and so on. Finally, it comes to the operation of the upper computer. First of all is to do correction of data channels. If calibration results are normal, the data acquisition can be launched. The overall diagram of CMOS image acquisition is shown in figure

VII, the PC display of acquisition system is shown in figure VIII.

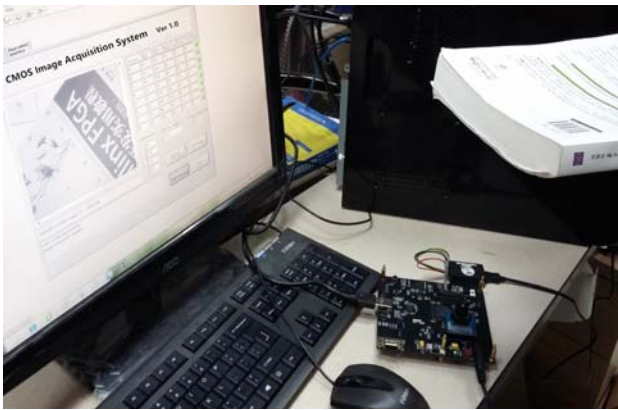


FIGURE VII. OVERALL DIAGRAM OF CMOS IMAGE ACQUISITION

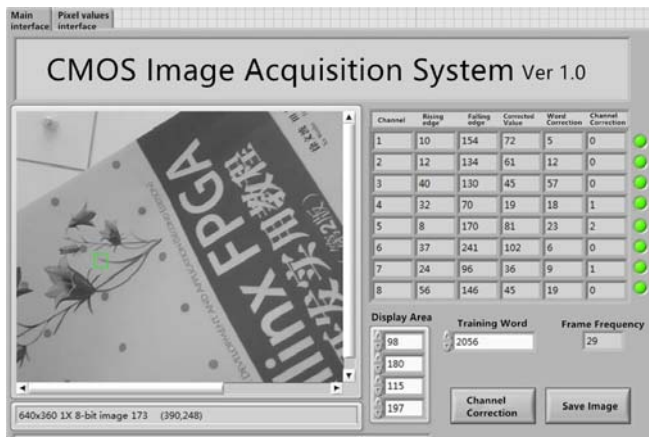


FIGURE VIII. PC DISPLAY OF ACQUISITION SYSTEM

V. CONCLUSION

The design in the paper is a high-speed data acquisition system used in CMOS image sensor, the system uses FPGA with strong parallel processing ability as the main control chip and DDR3 chip is responsible for the high-speed data cache or storage, and then uses the Ethernet for communication with PC. After testing, the system can carry on the image acquisition of CMOS image sensor. It can meet the requirements of large part of the acquisition. Another advantage of the system is very good flexibility, acquisition card is powered by 5 v dc power supply. The PC software designed with the Labview design can conveniently be repackaged into executable files, which makes the system gain a wide range of applications.

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