DPN Treatment plus Annealing Temperatures for 28nm HK/MG nMOSFETs with CHC Stress

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Abstract—The possible nano-crystallization formation and thicker interface layer at the higher annealing atmosphere, however, is easy to suppress the superiority of high-k dielectric deposition in the improvement of drive current and reliability. This phenomenon was apparently observed at 900°C annealing tested devices after the nitridation process. The drive current at 900°C annealing before hot-carrier stress is lower than that at 700°C with the same nitrogen concentration and the same feature sizes. After the hot-carrier stress test at 125°C ambience, the degradation of the threshold voltage shift at 900°C is still the worst among all of tested samples.

Keywords-hot carrier stress; drive current; high-k; MOSFET; anneal; metal-gate; DPN

I. INTRODUCTION

The shrinkage of MOSFET channel length and gate dielectric thickness at nano-node process causes more reliability problems if the recent nano-node process technology still follows the 0.13 m process generation. The gate leakage current increases rapidly when the gate oxide thickness with the growth of silicon dioxide is thinning more. Thus, with bringing in high-k (HK) material [1] as a gate dielectric to solve these former drawbacks is a suitable way. The hafnium-based high-k material $HfZrO_x$ [2] is one of most promising gate dielectric materials to replace SiO_2 or SiON due to its relatively high dielectric constant, less charge traps, lower interface states, more uniform film quality than pure HfO_2, higher nano-crystallization temperature, better thermal stability with silicon, and longer bias temperature instability (BTI) lifetime [3].

Recently, reliability issues of the hafnium-based dielectric such as positive bias-temperature instability (PBTI) and time-dependent dielectric breakdown (TDDB) inducing degradation [4] have been extensively investigated. Nevertheless, the channel hot-carrier (CHC) is also one of the main gate dielectric reliability issues. It has not yet been fully and systematically studied, especially the nitridation effect to device performance coming from decoupled plasma nitridation (DPN) process [5] after hot-carrier reliability stress on $HfZrO_x$ gate dielectrics. To investigate the basic electric characteristics and reliability characteristics with different annealing on hot-carrier injecting into HfZrOx dielectric layer, the CHC degradation test is made by different stress temperatures and operates on the n-channel MOSFET (nMOSFET) structures with three different channel lengths (L=1, 0.1 and 0.03 m).

II. BRIEF FABRICATION OF NANO-NODE DEVICES

One simple contour of a nano-planar MOSFET device to demonstrate the cross-sectional device under process fabrication is depicted in Fig. 1. The cardinal structures propose substrate, channel, source/drain (S/D), interfacial layer (IL), high-k with $HfZrO_x$ formation [6], barrier metal and low-resistivity metal gate. In order to promote the drive current in nMOSFET and pMOSFET, there are two strain technologies in nano-node process possibly adopted: stress memorization technique (SMT) and contact etch stop layer (CESL) process beneficial to nMOSFET device and embedded SiGe S/D plus replacement metal gate (RMG) technique helpful to pMOSFETs. Here is the choice with the latter for pMOSFETs in this work. The entire 28nm high-k/metal-gate (HK/MG) process flow with gate-last (GL) process is depicted in Fig. 2 [7].
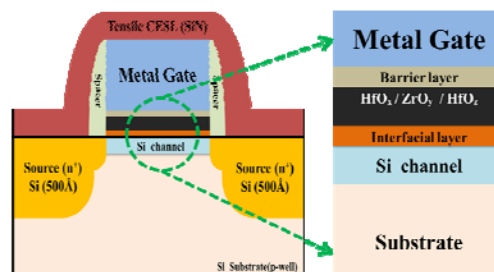

FIGURE I. SCHEMATIC CROSS-SECTION PROFILE OF AN NMOSFET

FIGURE II. SIMPLE PROCESS PROCESS FLOW FOR 28NM GATE-LAST MOSFETS

III. TEST RESULTS AND DISCUSSION

In this work, there were two experimental DPN treatment groups: different annealing temperatures (700°C and 900°C) in the nitrogen (N$_2$) concentration (<13%) atmosphere. One control group with post-deposition annealing (PDA) process in NH$_3$ and under 700°C annealing was also included. On the basis of the tested data, as shown in Fig. 3, the roll-up phenomenon of linear threshold voltage (V$_{t,lin}$) for nMOSFETs with the constant-current measurement before CHC stress was observed with various channel lengths on different nitridation annealing temperatures. But the V$_t$ of nMOSFETs should be reversely roll-off as the channel length scaling down according to the previous behaviors in the deep submicron process. For the above phenomenon, it may be explained by using halo implant process to increase threshold voltage and prevent short channel effect from the shrinkage of channel length. While the stress temperature is increased, the V$_t$ is decreased due to the possible repairs of interface state coming from the thermal energy on the channel surface.
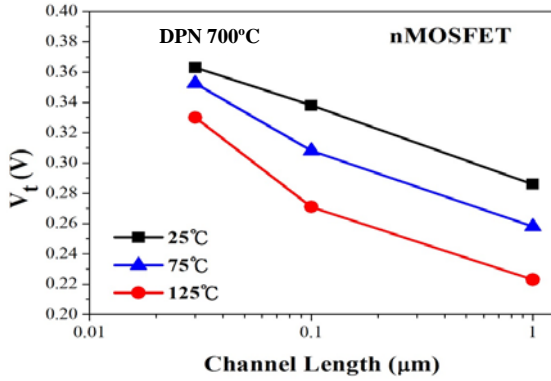

FIGURE III. LINEAR V$_{t,lin}$ VS. CHANNEL LENGTHS FOR PDA NMOSFETS UNDER TEMPERATURE STRESS AT 700oC ANNEALING TEMPERATURE

For a saturation drive current of an nMOSFET (I$_{DS}$), it can be expressed as [8]

$$I_{DS} = \frac{W}{2L} \mu_n \cdot C_{ox} \cdot (V_{GS} - V_t)^2 \cdot (1 + \lambda \cdot V_{DS}) \qquad (1)$$

where μ_n: channel mobility, C$_{OX}$: gate capacitance with unit area and : channel-length modulation factor. To increase the C$_{OX}$, the high-k gate dielectric is adopted into the advanced nano-node process fabrication. The V$_t$ value can be given as

$$V_t = \Phi_{ms} - \frac{Q_f}{C_{ox}} - \frac{Q_d}{C_{ox}} + 2\phi_F \qquad (2)$$

where $_{ms}$: work function difference between gate and Si substrate, Q$_f$: fixed charges in gate insulator or interface states between silicon surface and interfacial layer, Q$_d$: depletion charges in surface channel, and q$_F$: E$_i$ (intrinsic Fermi level)–E$_F$ (Fermi level).

In the reliability test, the influenced device parameters chiefly relate to trapping or de-trapping generation on the channel surface or in the gate dielectric. The common discussion focuses on the ON current, V$_t$, G$_m$, sub-threshold swing (SS), and device leakage. The trans-conductance G$_m$ is a good index to probe the interface quality distributed at the channel surface. For a drain current operating at the linear region, it can be expressed as (3) and the G$_m$ at the fixed V$_{DS}$ can be given as (4)

$$I_{DS,lin} = \frac{W}{L} \cdot \mu \cdot C_{OX} \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) \cdot V_{DS} \qquad (3)$$

$$G_m = \frac{\partial I_{DS}}{\partial V_{GS}} |_{V_{DS}=0.05V} = \frac{W}{L} \cdot \mu \cdot C_{OX} \qquad (4)$$

When we discuss the device performance, the parameter, subthreshold swing (SS), should be introduced due to the index of interface quality and the off-leakage such as gate-induced drain leakage effect as well as the switching quality for this device. The SS can be defined as

$$SS = 1000 \left(\frac{d \log(I_{DS})}{dV_G} \right)^{-1} = 2.3 \frac{kT}{q} \left(1 + \frac{C_d + C_{it}}{C_{ox}} \right) 1000 \qquad (5)$$

where k: Boltzmann constant, T: absolute temperature, C$_d$: depletion capacitance in channel surface, and C$_{it}$: equivalent interface-state capacitance. The unit of SS is mV/decade.

Before the stress, the initial characteristics of drive currents with channel lengths (L=0.03, 0.1, and 1μm) as channel width W= 1μm are exhibited in Fig. 4. The difference of ON current at L=1μm is specially illustrated in Fig.5. The tested devices with different treatment temperatures in nitridation demonstrate the similar performance for the long-channel devices, but the drive current with PDA nitridation is gradually better than the others as the channel length is shortened due to the contribution of Si-H bonds on the channel surface. This evidence also shows in Fig. 6. Lower interface state; higher channel mobility.
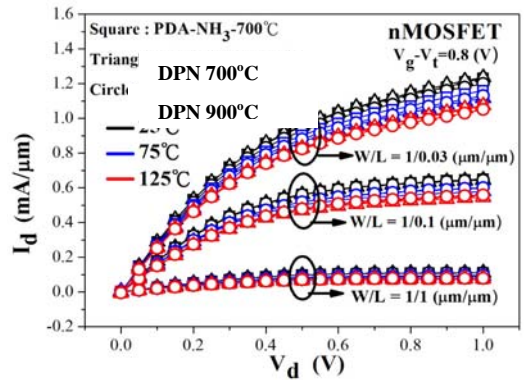

FIGURE IV. DRIVE CURRENTS WITH DIFFERENT TESTED DEVICES AT 25, 75, AND 125oC

However, as the stress temperature is increased, the channel scattering is also increased, inducing the degradation of channel mobility proved by the trans-conductance (G_m) results with W/L=1/0.03 (µm/µm), as shown in Fig. 6. The whole variation with different tested devices at the maximum G_m (G_{m_max}) is shown in Fig. 7. While the channel length is longer, the G_{m_max} is not easily influenced by the increase of temperature. Because of the increase of the degradation amount if they are similar, the impact to the degradation of the drive current is not serious. The change of G_{m_max} at the long channel device is relatively small. On the contrary, the impact is increased in contrast to the short channel device.
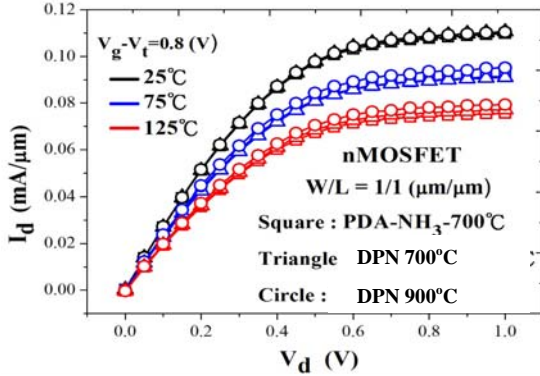

FIGURE V. DRIVE CURRENTS WITH W/L=1/1 (µm/µm) AT 25, 75, AND 125oC

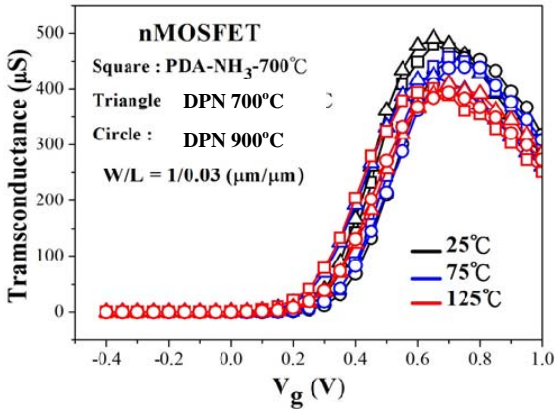FIGURE VI. ILLUSTRATION OF Gm WITH W/L=1/0.03 (µm/µm) AT 25, 75, AND 125oC

When the V_t change is seen, as shown in Fig. 8 and 9, the cardinal dominant is the fixed charge usually related to the number of interface state (N_{it}) by unit area, oxide trap (N_{ot}), or both, as shown in Fig. 10. Because the hot carrier stress impacts the shorter device more, we focus on the tested device with W/L=1/0.03 (µm/µm). At room temperature, the maximum V_t shift is with DPN 700°C condition. The V_t shift with DPN 900°C is the minimum, as shown in Fig. 8. However, the case at 125°C stress is fully reversed, as shown in Fig.9, due to the increased degradation of channel mobility, illustrated in Fig. 6. The CHC stress condition was the stress voltage V_{stress}= 1.4V_{cc}+V_t as V_{cc}=0.8V, V_g= V_d= V_{stress} and V_b=V_s= 0 V as well as the stress temperatures 25, 75, and 125

°C. After 3000s CHC stress, the V_t shift of the tested devices with different annealing temperatures will be exposed more.

According to (5), the difference of C_{it} = q D_{it} before and after stress can be extracted as [9].
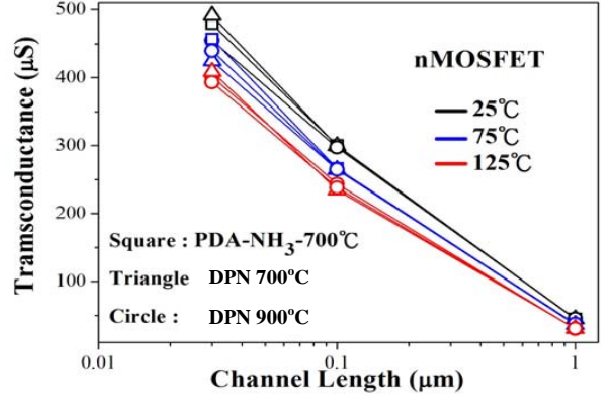

FIGURE VII. MAXIMUM Gm WITH CHANNEL LENGTHS AT 25, 75, AND 125oC

$$N_{it} = \int_{E_V}^{E_C} D_{it} \cdot dE \approx D_{it} \cdot E_{it}$$

(6)

$$\Delta N_{it} = \frac{\Delta SS \cdot C_{OX} \cdot E_{it}}{2.3 \cdot kT \cdot 1000}$$

(7)

where D_{it}: interface state density and E_{it} : (E_i - E_F).

The fixed charges in device are probably classified as N_{it} and N_{ot}, excluding the mobile ion contribution. The total change of charge number N_{tot} is basically equal to (N_{it}+ N_{ot}).

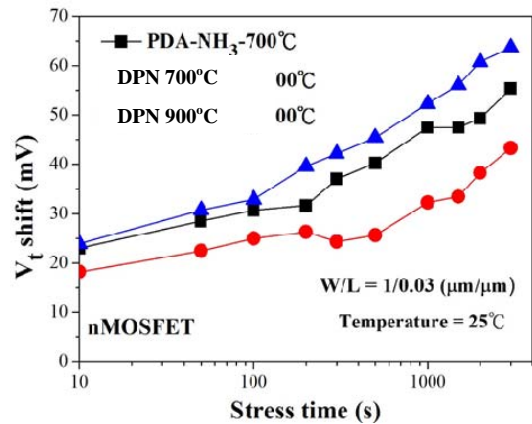$$\Delta N_{tot} = \frac{\Delta V_t \cdot C_{OX}}{q}$$

(8)
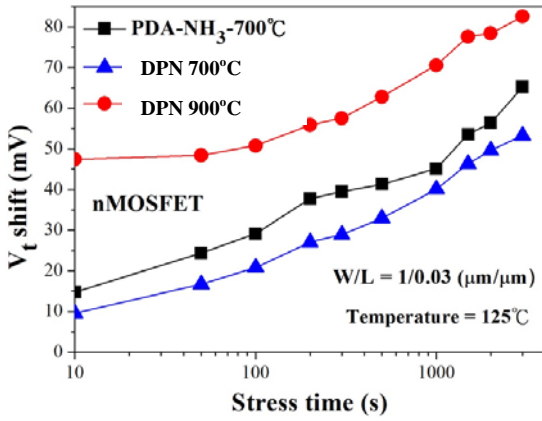

FIGURE VIII. V_t VS. STRESS TIME AT ROOM TEMPERATURE
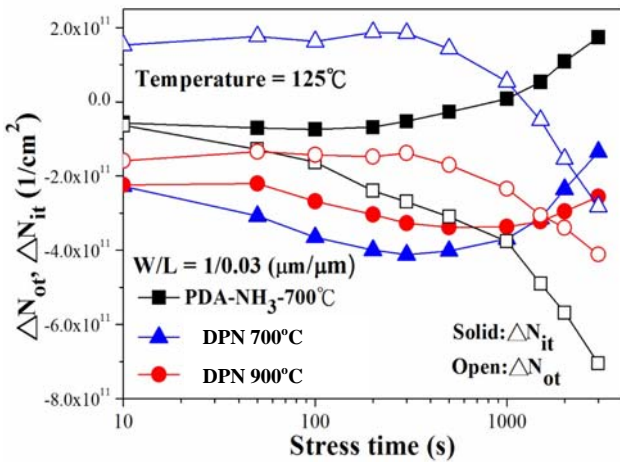
FIGURE IX. V_t VS. STRESS TIME AT 125oC.
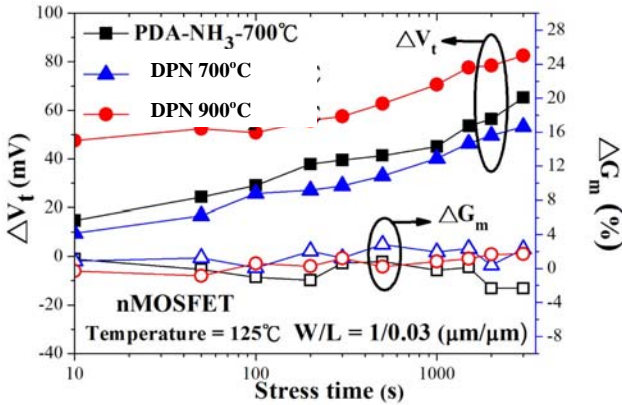

FIGURE X. DISTRIBUTION OF $\triangle N_{IT}$ AND $\triangle N_{OT}$ VS. STRESS TIME

FIGURE XI. V_t SHIFT AND G_m CHANGE VS. STRESS TIME AT 125oC

In Fig. 10, the trends of $\triangle N_{it}$ and $\triangle N_{ot}$ are not consistent in stress. For the PDA 700°C condition, the hole trapping for $\triangle N_{it}$ dominating at the short-time stress gradually moves to the electron trapping, related to the Si-H bonds in generation and recombination amount. However, the trend of $\triangle N_{ot}$ is always dominated by the hole trapping. For the DPN 700°C, the hole trapping amount for $\triangle N_{it}$ initially increases, but the change happening when the stress time is increased more due to the increase of the impact ionization. Reversely, the electron

trapping for $\triangle N_{ot}$ shows the stronger influence in the initial stage, but the hole trapping impact is increased as the stress time is increased due to more hole carriers trapped into gate dielectric. For the DPN 900°C, the trend of $\triangle N_{it}$ keeps at the hole trapping mechanism and so does the $\triangle N_{ot}$, but the amount of $\triangle N_{ot}$ is raised. However, the variation of $\triangle N_{it}$ and $\triangle N_{ot}$ at DPN 900°C seems not more serious than that at DPN 700°C.

In this study, the shortest-channel tested device after CHC stress represents the largest V_t shift with DPN 900°C annealing. This effect may be attributed to the higher anneal temperature causing the possible nano-crystallization dielectric and indirectly influencing the device performance in reliability consideration. The dominant factor in degradation should be oxide trap because Fig. 11 provides the evidence illustrating the G_{m_max} shift (%) is not huge no matter what the nitridation treatment is. The distribution profiles of trans-conductance for all before and after test are similar.

IV. CONCLUSION

Nitrogen plasma is indeed a good recipe to fix the vacancy or oxide trap in high-k gate dielectric. However, the unsuitable control in nitrogen concentration and annealing temperature will degrade the device performance, not only in the initial stage, but in reliability consideration. Using the lower annealing temperature (700°C) is a good choice to promote the device performance and represent the lower reliability suffering after the CHC stress. As the stress temperature is increased, the degradation of device performance is distinctly raised due to the extra thermal energy providing more phonon scattering as well as the generation of electron-hole pairs on the channel surface. Basically, The changes of N_{it} and N_{ot} dominate the degradation of channel integrity. In this work, N_{ot} seems the main role influencing the degradation in device performance, especially in V_t shift. At the higher temperature stress, the DPN 900°C shows the maximum degradation in V_t shift probably attributed to the nano-crystallization in gate dielectric. Next, higher annealing temperature; easily increasing thicker interfacial layer and reducing the k-value in gate dielectric.

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