Research on Chip Cooling of High Power Density Integrated

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***Abstract*—Increasingly, heat flux density on one chip reached to 1KW/cm^2 with the development of integration technology. However, it is hardly to meet the demand of 417K for conventional cooling way. Chip cooling become the bottleneck of integration further. This paper put forward that integrated micro channel in the chip, through which the micro fluid could transfer internal heat to the external. According to the actual working conditions, entrance flow speed and temperature could be adjusted to ensure the normal work of the chip. Firstly, analog chips model including unknown size micro channel was designed. Secondly, the ANYSIS software was adopted to find the proper size. Moreover, size 40μm micro channel could satisfy the high temperature on chip was 413K approximately. Furthermore, the situation of bi-direction flow, changed entrance velocity and entrance temperature was considered to reach the optimized result. It indicated that the chip cooling with micro-channel was feasible.**

Keywords-micro-channel; integrated chip cooling; the numerical simulation; micro-fluidic

I. INTRODUCTION

With the enhancement of the function, the number of transistors integrated in a single chip was increased sharply. In 2006, International Technology Roadmap for Semiconductors (ITRS) projects had suggested that the power density of the single chip will be by 60 - 80W/cm^2 improve to 108W/cm^2 by 2018[1]. However, 3D chip apparently had broken the human imagination about technology development, since a plurality of high power density chip package in an single chip produced hot spot area with high heat flux density in 2008[2-3]. In 2013, the national defense pre research plan bureau (DARPA) released to the industry on a project named "Inner Chip/Chip Enhanced Cooling" (ICECool), which aimed at cooling chip with heat flux density 1KW/cm^2, heat energy density to 1KW/cm^3. Undisputedly, the maximum operating temperature of the chip is 413 K, the chip would lost its function because of high temperature gradient if operating temperature was higher[4-6]. Therefore, chip cooling had become the bottleneck of further improving the integration. It limited to improve the level of integration, reduce the size of chip, increase the system function continuously. Therefore, academic research paid more attention on this problem[7-10].

On the basis of previous studies, this paper proposed a chip inner cooling method which integrated micro-channels in a chip. When micro-fluidic pass through the micro-channels, the thermal could be taken out from chip. Through the numerical simulation, the feasibility of ideas would be confirmed. Moreover, the numerical simulation method also was used for micro-channel size selection. During design, hot spots and micro-channels was taken as hot area to ensure the whole temperature below 417 K.

II. HIGH POWER DENSITY INTEGRATED MICRO-CHANNEL SIMULATION CHIP MODEL DESIGN

The chip integration degree is higher and higher and the chip size is smaller and smaller, its internal thermal power density reaches 1KW/cm^2. In this paper, we focused more on chip cooling effect rather than a circuit function. MEMS technology was adopted to realize the integration of the micro-channel chip. It is necessary to consider the following factors: (1) The chip material, structure and the overall size; (2) The generation of heat and temperature detection; (3) the micro-channel overall design, including the entrance, exit and gateway; (4) the size of micro-channel.

(1) As to chip material problem, it was needed to consider the actual situation. At present, silicon was taken as basic material of large scale integrated circuit chips. Meanwhile, thermal conductivity of silicon was higher than other non-metallic materials. Thus, silicon was taken as the main material of integrated simulation chip. Further, glass was taken as the other material because of facilitating micro-channel entrance and exit. Silicon base and glass base constituted integrated chip structure. The reference of commonly chip packaging size was 10mm*10mm*0.9mm. Comprehensively MEMS processing technology, silicon base design thickness was 130 μ m and glass base thickness was 500 μ m. Silicon base and glass base were etched 80 μ m depth micro-channel respectively. Then they were put together by the anodic bonding, in order to simulate the function of power density integrated micro-channel chip cooling. The simulation chip model diagram was shown in Fig.1.

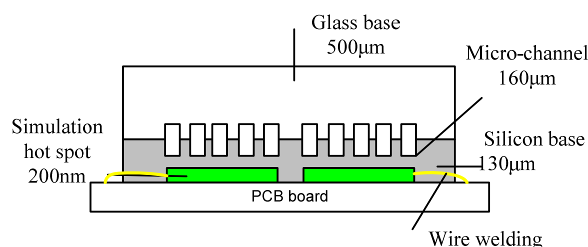

FIGURE I. SCHEMATIC DIAGRAM OF INTEGRATED MICRO-FLUIDIC CHIP

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(2) Ignoring the circuit function, it is necessary to embed heater inside the simulation chip. Considering all kinds of heater, platinum could be used to generate heat and detect temperature. 200 nm thickness platinum was sputtered silicon base surface to simulate hot spot, 200 um width platinum as lead-wire through the silk fiber welding technology to the outside peripheral PCB board. Two hot spots made from 10 μ m width platinum wire coil bending to simulate, each size was 2000 μ m*200 μ m*200 nm and the thermal power was up to 4W, and thermal power density reached $1KW/cm^2$. Simulated hot spots size and shape diagram was shown in Fig.2.

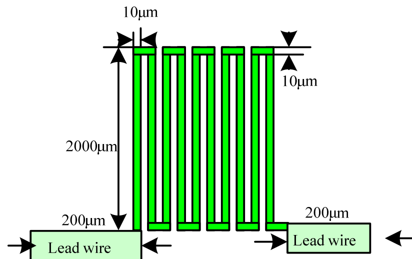


FIGURE II. SIMULATION HOT SPOTS DIAGRAM

(3) Micro-channel was designed on the bonding surface of the glass base and silicon base, it included micro-tank, entrance of micro-fluid, entrance of micro-fluid, micro-channel and micro-channel gap. With the 1.6mm diameter tube, micro-fluid was pumped into micro-tank through entrance, flowed through the micro-channel into micro-tank, finally pumped outside from exit. To facilitate processing, entrance and exit of micro-fluid designed on the glass base, as shown in Fig.3.

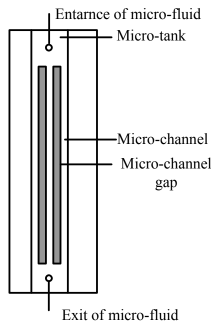


FIGURE III. MICRO CHANNEL STRUCTURE SKETCH DIAGRAM

(4) Combined hot spots and the bottom of the micro-channel with the same area, hot area was constituted. It is necessary to decrease the highest temperature on the hot area below to the required temperature. The size of the micro-channel should be designed on the basis of numerical simulation results.

III. NUMERICAL SIMULATION OF INTEGRATED MICRO-CHANNEL CHIP COOLING

A. *Numerical Simulation of Assumptions and Boundary Conditions*

Micro-channel wall of silicon surface was heat conduction while glass surface was isothermal adiabatic. Silicon thermal conductivity was 138.5 W/(mK) and the glass was 0.93 W/(mK). It was assumed that fluid-structure interaction surface was no velocity slip. The micro-channel substance was deionized water. Under normal circumstances, density of deionized water was unchangeable with the change of temperature and pressure. That could be assumed as a constant. Moreover, expansion in liquid was small, could be ignored. To make the following assumptions and simplified model in the numerical simulation:

(1) Micro-fluidic was certain physical properties and steady flow;

(2) Heat radiation and air natural convection of chip was ignored, and the outer surface of the silicon and glass was assumed insulation;

Boundary conditions are set as follows:

(1) The heat transfer from the surface between simulation hot spots and silicon base was from solid to solid, while the heat transfer form fluid-structure interaction surface was from solid to fluid;

(2) The outside wall of hot spots as the adiabatic surfaces;

(3) The micro-fluid entrance was set to fluid speed, exit was set to free opening;

(4) The hot spots was set as a source of body heater source (heat flux density was $1KW/cm^2$).

B. *The Geometric Model*

Integrated micro-channel chip geometry model was build in the UG software. In order to express the temperature changing accurately and clearly, the three-dimensional structure model was adopted in this paper, as shown in Fig.4. Due to two simulated hot spots was the same exactly, only one hot area was numerical simulation in the integrated chip model. Integrated chip core size was 2mm*2mm*0.63mm, while hot spot was 2000 um *200 um * 200 nm. Which heat power was up to 4W. Micro-channel was designed in different sizes, the depth was 160 μm. The spacing between micro-channel was 40 um, the depth was 160μm. This structure was consisted of silicon base and glass base double-layer structure. The area of 2000 um *200 um * 200 nm was cut as the hotspot on the silicon base. Micro-fluidic channels was cut from silicon base and glass base, including micro-tank, entrance and exit. Obviously, geometric model of integrated micro-channel chip was the same as physical model completely.

Six cases was numerical simulation in this paper. Where, Case-A: four 20 μm micro-channels; Case-B: three 30μm micro-channels; Case - C: three 40 μm micro-channels; Case-D: three 50 μm micro-channels; Case-E:two 60μm micro-channels.

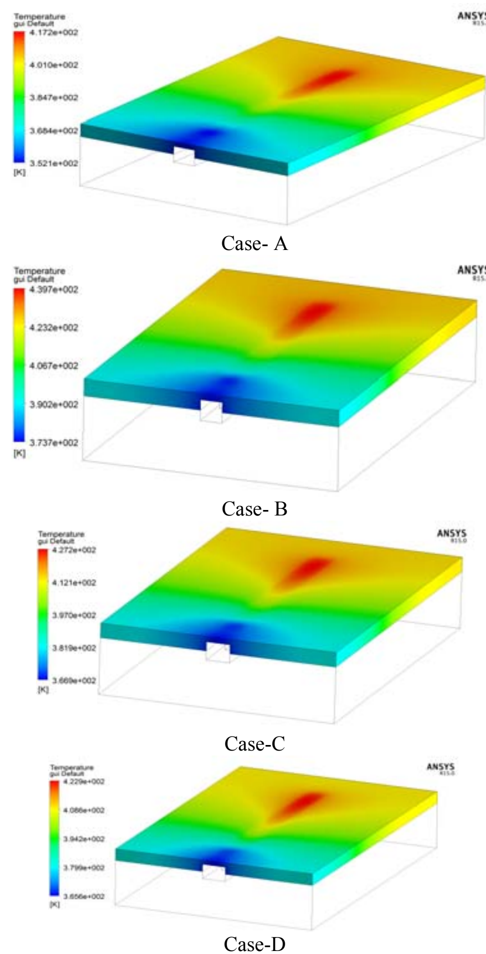
C. *Numerical Simulation Method*

Currently, the main micro-fluid numerical simulation methods were continuous medium model, molecular model and mesoscopic simulation method. As to chip cooling, micro-fluid flow should be maintain continuity to ensure the continuity of cooling.

During numerical simulation, using continuity equation and the Globe Dynamic Model, the heat power were defined as (1.574 e+11) W/m^3, entrance flow speed were given as 0.3 m/s, the initial temperature were set to 293K, the exit was set to opening. based on it, different size of micro-channel were numerical simulated, such as Case-A, Case-B, Case-C and so on. It was necessary to choose micro-channel which could meet both temperature control requirement case and the MEMS processing technology. In order to optimize effect, numerical simulations were executed in different entrance velocity, different flow direction and different entrance temperature. The aim of simulation was to provide theoretical guidance for later experiment.

IV. THE RESULTS OF NUMERICAL SIMULATION AND ANALYSIS

Adopted setting conditions above, the iteration of the temperature field was continued until the model converged. Where, temperature distribution on silicon surface results were shown in Fig.4.



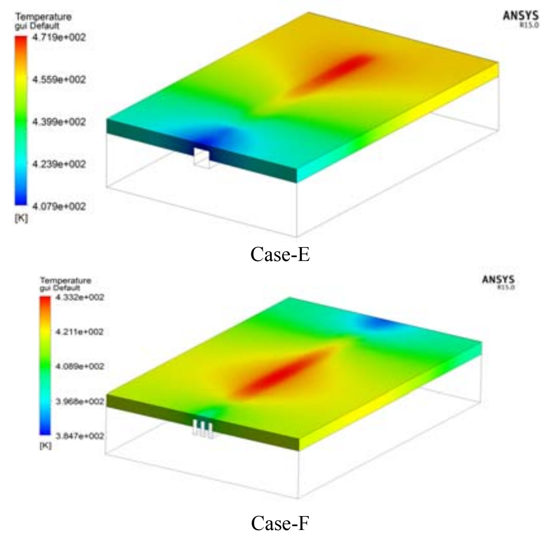


FIGURE IV. THE RESULTS OF NUMERICAL SIMULATION OF TEMPERATURE DISTRIBUTION ON THE SILICON SURFACE BASE

Where, the highest temperature were 417 K, 439.7 K,427.2 K, 422.9 K , 471.9 K from Case-A to Case-E respectively. The temperature distribution of the results showed that, in the same hot area, the finer micro-channel, the more quantity micro-channel, the better cooling effect was achieved. Obviously, it is consistent with the theoretical analysis. As to Among MEMS processing technology, the more width of the micro-channel, the higher the success rate of the process. Therefore, the result of Case-D could meet both required temperature and MEMS processing technology. It was chosen to carry out optimization strategy further.

During cooling, micro-fluid passed through the fluid-structure interaction surface, transferred heat away by heat convection. At the same time, it own temperature was raised. At the exit, heat exchange performance of micro-fluidic became poor since the temperature difference between micro-fluidic and hot spot was very small. Therefore, the temperature peak was appeared at the micro-fluid exit. That means micro fluid heat transfer performance was negatively related to the micro fluid temperature. What about bi-directional flow? Would it make the highest temperature dropping? Based on the Case-D, micro-fluidic bidirectional flow numerical simulation was completes. In this case, there were three micro-channels in the chip. In both sides of the micro channel, micro-fluidic flowed from the right to the left. Meanwhile in the middle of the micro channel, micro-fluidic flowed from the left to the right. The simulation result was showed in Case-G in Fig.5. Compared with Case-D, the highest temperature area moved to the center. However, the red high temperature area was larger and the highest temperature was higher apparently, which was up to 433.2 K. This was different from assuming. Reason lied in two aspects, on the one hand, micro-fluidics was dispersed to two-way, the temperature raised faster. Further, increased temperatures decreased heat exchange ability. On the other hand, heat transfer phenomenon was appear because of bidirectional micro-fluid different temperature. Eventually,

larger high temperature areas and worse heat transfer effect were formed.

V. CONCLUSION

In this paper, a high heat flux integrated micro-channel cooling chip was designed. It proposed cooling model for the 1 KW/cm2 heat flux density. On the basis of previous studies, chip structure of silicon based and glass based anodic bonding was design. Sputtering platinum to simulated heat which was produced during circuits work, the chip was closed to real chip. The hot region was consisted of hotspots which heat flux density was up to 1KW/ cm^2 and area was 2000μm*200μm*200nm. Micro-channel which width was from 20μm to 60μm was designed on bonding face to realize the function of heat transfer. Then ANYSIS software was adopted to find the proper size. Where size 40μm micro channel could satisfy the high temperature on chip was 413K approximately. Moreover, bi-directional flow, different velocity and different micro fluid entrance temperature were considered in simulation. Furthermore, The simulation results showed that this method was effective to fulfill the cooling function.

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