FMECA for LRM based on Degradation Data

Chen Ran[1,2 a], Lian Guangyao[2,b] ,Geng Mengxue[2,c],Li Baochen[1,d],Cai Liying[2,e]

[1]Mechanical Engineering College, Shijiazhuang 050000,China

[2]New Technological Research Institute,Shijiazhuang 050003,China

[A]email:Interran@126.com, [b]email:ddgcx@126,
[c]email:499951453@qq.com,[c]email:Baochen_Li@163.com,[c]email:cailiying@sina.cn

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Abstract. Failure Mode Effect and Critically Analysis(FMECA) is one of the key technologies in testability verification test that based on plenty of failure samples.Line replaceable module(LRM) is the core of the new generation avionics system and military equipment electronic system. Failure data of LRM is difficult to acquire under natural conditions,however,it could be obtained fleetly through accelerated degradation test(ADT).According to the degradation data obtained from the accelerated degradation test and the degradation model, the typical failure modes and the occurrence probability of the LRM could be obtained.

Introduction

FMECA, as one of the key technologies in testability verification test, is based on failure samples. FMECA is usually realized through hardware and function analysis. .In verification and evaluation tests,FMECA is utilized to identify all possible failure modes, which can be selected as samples of tests[1,2]. According to the statistics of the U.S. Military, the failure rate of electronic equipment is 55% caused by temperature[3].Heat radiating problem of LRM is more serious than that of traditional electronic products due to its complete package and highly integrated circuit, which may lead to typical failure modes and the change of failure rate.However,failure data of LRM is difficult to acquire spontaneously due to its high reliability.

Accelerated Degradation Test(ADT) has the advantage of reducing time to obtain adequate failure samples in the study of reliability issues related to degradation failure. In this paper, typical failure modes are identified and failure rates are recalculated by ADT, as a result, the blindness in FMECA for LRM could be eliminated.

Analysis of LRM Structure Characteristics and Circuit Working Environment

There are several military or commercial standards issued internationally such as SEM-E， ARINC650， VITA48， ASAAC and so on that rules the interface and design specifications of LRM in mechanical, electrical and communication[4,5].According to the above standard, it can be known that LRM has a strong package shell.LRM is closely counted on the mounting frame and connected with the circuit of the system through the back board.This kind of system has a quite compact structure, but not conducive to heat dissipation.What’s more, highly integrated large-scale ultra high speed circuit is usually a three-dimensional integrated circuit, which can reduce the circuit size and wire length, but might lead to very high power density and heat flux, and local overheating area of the module circuit.Due to the complexity of the structure of the integrated circuit, even if with a good thermal design, the problem of stress concentration caused by temperature factor is still inevitable.

Failure analysis based on degradation model

Degradation model of electronic equipment. Degradation model is a mathematical model to describe the failure law of product degradation.The reliability index of the products including the failure probability required by FMECA could be obtained by utilizing the degradation model to deal with the failure data[6,7].Let $\mathrm{y}(t)$ be the degradation at t moment , define l as failure threshold.Failure is believed to occur when $\mathrm{y}(t) \ge l$. $F(t) = P(\mathrm{y}(t) \ge l)$ is the product failure probability. The degradation process is uncertain which could be described by random process.Set the one dimensional

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distribution of the degradation $y(t)$ at t moment down as $G(y,t)$,whose probability density function is denoted as $g(y,t)$ .Obviously,there is $\int_{-\infty}^{+\infty} g(y,t)dt = 1$ .For the same object, if the failure mechanism does not change, the distribution of the degradation would not be changed. The normal distribution, Weibull distribution and Gamma distribution are commonly utilized to describe the process of product degradation.The relationship between the failure occurrence probability and the degradation process of the product is shown in the Eq.1.

$$F(t) = P(y(t) \geq l) = 1 - G(l,t) \tag{1}$$

Degradation failure of electronic equipment is often due to the degradation of components.The degradation failure of components is the physical or chemical processes such as corrosion, electro-migration and insulation failure.And the temperature factors affects the degradation failure of components by affecting the movement of electrons, chemical reaction rate and so on. Aiming at degradation of product performance due to temperature degradation, the Arrhenius equation is presented by Arrhenius' research in nineteenth Century to characterize the relationship between the performance degradation rate of the electronic equipment and the temperature stress[8].The Arrhenius equation is shown in Eq.2.

$$m(T_j) = \frac{dx(T_j, t)}{dt} = A\exp(-\frac{E_a}{kT_j}) \tag{2}$$

While $m(T_j)$ is also referred to as the degradation drift coefficient of the stress T_j, T_j reflects the temperature level，Ea(eV) is the activation energy, And $k = 8.6171 \times 10^{-5}$ is the Boltzmann constant.

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Failure Analysis Based on ADT data. According to the test data obtained by ADT, the typical failure modes of LRM under degradation stress could be identified.However, the occurrence and other information should be taken into further analysis based on the degradation model[9].The degenerate law of the sample is assumed to obey the normal distribution process,so that the degradation follows normal distribution, which could be shown in Eq.3.

$$f_{i,i-1} = \frac{1}{s\sqrt{2p\Delta t}}\exp[-\frac{(x_i - x_{i-1} - m\Delta t)^2}{2s^2\Delta t}] \tag{3}$$

While x_i and x_{i-1} are the performance measured value of the test piece at i and i-1times, Δt is the time interval between two measurements, m is the drift coefficient shown as the degradation drift coefficient of the stress T_j in Eq.2, $s > 0$ 为is the diffusion coefficient,whose value does not change with T_j.If set $y = 0$ when $t = 0$,there would be Eq.4：

$$g(y,t) = \frac{1}{s\sqrt{2pt}}\exp[-\frac{(y - mt)^2}{2s^2 t}] \tag{4}$$

Supposing there are m samples taking ADT under k temperature levels，and each subject measured n times， m and s could be solved out by maximum likelihood estimation method.Likelihood function is shown in Eq.5：

$$L = \prod_{j=1}^{k}\prod_{l=1}^{m}\prod_{i=1}^{n} f_{jli,jl(i-1)} \tag{5}$$

Solving out the natural logarithm of Eq.5,then let partial derivative of m and s be 0.There would be Eq.6 & Eq.7.The results would be shown as Eq.8 after Solving out the natural logarithm of Eq.2.Take $m(T_j)$ and $1/T_j$ solved in Eq.6 into Eq.8,values of A and Ea could be solved out by the utilizing of the least square method as shown in Eq.9 & Eq.10.Set T_{U0} be the The temperature of the sample during the LRM circuit operating.Drift coefficient of performance degradation $m = m(T_{U0})$ under T_{U0} could be obtained by taking A and Ea into Eq.2. Finally, the failure probability $F(t)$ under T_{U0} could be solved out according to Eq.1 and Eq.4：

$$m(T_j)=\frac{\sum_{l=1}^{m}\sum_{i=1}^{n}(x_{j,l,i}-x_{j,l,i-1})}{\sum_{l=1}^{m}\sum_{i=1}^{n}(t_{j,l,i}-t_{j,l,i-1})} \tag{6}$$

$$s^2=\frac{\sum_{j=1}^{k}\sum_{l=1}^{m}\sum_{i=1}^{n}\frac{(x_{j,l,i}-x_{j,l,i-1}-m(T_j)(t_{j,l,i}-t_{j,l,i-1}))^2}{t_{j,l,i}-t_{j,l,i-1}}}{kmn} \tag{7}$$

$$\ln m(T_j)=\ln A-Ea/KT_j \tag{8}$$

$$Ea=-K\frac{k\sum_{1}^{k}\ln\frac{m(T_j)}{T_j}-\sum_{1}^{k}\ln m(T_j)\sum_{1}^{k}\frac{1}{T_j}}{k\sum_{1}^{k}(\frac{1}{T_j})^2-(\sum_{1}^{k}\frac{1}{T_j})^2} \tag{9}$$

$$\ln A=\frac{\sum_{1}^{k}\ln m(T_j)+Ea/K\sum_{1}^{k}1/T_j}{n} \tag{10}$$

$$F(t)=1-\int_{-\infty}^{l}\frac{1}{s\sqrt{2pt}}\exp[-\frac{(y-m(T_{U0})t)^2}{2s^2t}]=1-f(\frac{l-m(T_{U0})t)^2}{s\sqrt{t}}) \tag{11}$$

In Eq.11, f indicates the standard normal distribution, and l indicates the failure threshold.

Case Study

A LRM named module A with control function is utilized as an example. Module A is the core of a control execution system in which data transfer with the superior computer and information interchange with the subordinate computer could be achieved, so that logical relation processing as well as state control and detection of the whole control execution process could be successfully implemented.The functions of the UUT is shown by Fig 1.

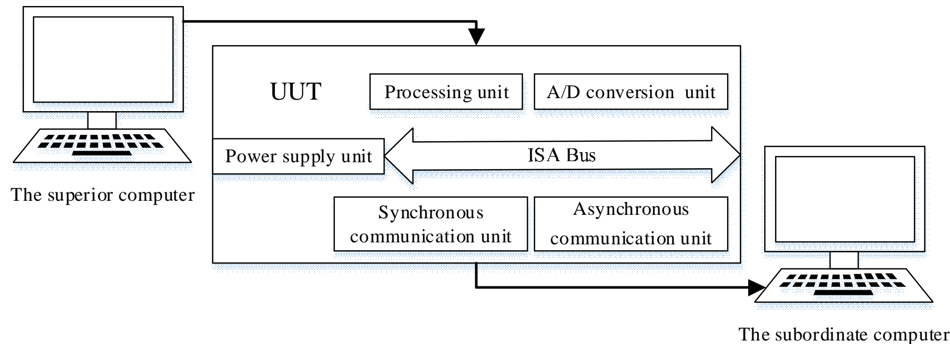

Fig 1 Function block diagram of the UUT

There are 3 main functional units in the UUT, including power supply unit, module support unit and processing unit. While in the power supply unit, the input large voltage DC power supply can be converted to +5V, +12V and -12V power supply required for each functional unit. There is a processor in the processing unit in which data processing, logic relation processing and state control could be realized. Module support unit including A/D conversion function unit and asynchronous / synchronous communication function unit that can provide support and implementation for the processor and Build-in-test(BIT) circuit.

A/D conversion function unit in module A is taken as the example in the case indicate whose FMECA worksheet provided by the manufacturer is shown in Table 1.

Table 1 FMECA for A/D conversion function unit

Unit	Function	Failure Mode	Failure Cause	Failure Effect	ESR	OPR	P_m(%)	RPN
A/D conversion function	Detect the power supply for device control line in execution system	Decoding controller chip damage	Over current or over voltage	Cannot achieve the correct decoding control function	3	6	0.961	18
		A/D conversion chip damage	Over current or over voltage	Cannot carry out AV to DV conversion	3	5	0.095	15
		D/A conversion chip damage	Over current or over voltage	Cannot carry out DV to AV conversion	3	5	0.095	15
		Isolation amplifier chip damage	Over current or over voltage	Cannot isolate the input voltage	3	7	2.856	21
		Analog switch chip damage	Over current or over voltage	Cannot achieve the multiple switched input function	3	6	0.421	6

The weak links and whose working temperature of module A are shown in Table 2.

Table 2 Weak link and working temperature

Weak links	Ceramic capacitor	Decoding controller chip	A/D conversion chip
working temperature	333K	348K	357K

Then the test data shown in Table 5 could be obtained by ADT.While,sample 1 is ceramic capacitor, sample 2 is Decoding controller chip, sample 3 is A/D conversion chip.Take the test data shown in Table 3 into Eq.4-Eq.7, and the drift coefficient $\mu(T_j)$ as well as the diffusion coefficient σ2 could be solved out.The value of A and Ea could be solved out by the utilize of Eq.9 and Eq.10, so that there would be: $Ea = 6.333\times10^{-2}$ $A = 2.526\times10^{-6}$ .Finally, taking the working temperature T_{U01}、T_{U02}、T_{U02},l=1,and σ of each sample into Eq.11, so that the failure modes and their occurrence probability related to temperature factor when the module is operating could be obtained.The above are shown in Table4.In summary, FMECA worksheet based on ADT could be obtained as shown in Table 5.

Table 3 Accelerated degradation test data

Stress Level	Sample number	Performance degradation & measurement time		
		1	2	3
343K	1	5.23	5.27	5.32
	1	5.27	5.33	5.37
363K	2	4.08	4.1	4.16
	3	4.06	4.11	4.14
	1	5.34	5.39	5.47
378K	2	4.09	4.13	4.19
	3	4.08	4.12	4.17

Table 4 Horizontal drift coefficient and diffusion coefficient

Subject	Ceramic capacitor	Decoding controller chip	A/D conversion chip
Working temperature	333K	348K	357K
$\mu(Tj)$	2640×10^{-4}	2.950×10^{-4}	3.147×10^{-4}
σ^2		1.600×10^{-6}	
occurrence probability%	1.782	1.274	0.324

Table 5 FMECA for A/D conversion function unit based on Accelerated Degradation Test

Unit	Function	Failure Mode	Failure Cause	Failure Effect	ESR	OPR	P_m(%)	RPN
A/D conversion function	Detect the power supply for device control line in execution system	Decoding controller chip damage	Over current or over voltage excessive local temperature	Cannot achieve the correct decoding control function	3	7	1.782	21
		A/D conversion chip damage	Over current or over voltage excessive local temperature	Cannot carry out AV to DV conversion	3	6	0.324	18
Unit	Function	Failure Mode	Failure Cause	Failure Effect	ESR	OPR	P_m(%)	RPN
A/D conversion function	Detect the power supply for device control line in execution system	D/A conversion chip damage	Over current or over voltage	Cannot carry out DV to AV conversion	3	5	0.095	15
		Isolation amplifier chip damage	Over current or over voltage	Cannot isolate the input voltage	3	7	2.856	21
		Ceramic capacitor damage	excessive local temperature	Output signal interference	2	7	1.274	14
		Analog switch chip damage	Over current or over voltage	Cannot achieve the multiple switched input function	3	6	0.421	18

Discussions

In Table 5, there is a typical failure mode in module A such as the ceramic capacitor damage when taking the temperature factor into consideration.The occurrence probability of whom that happen to be in the overheated zone are higher than expected.FMECA based on degradation data can quickly identify typical failure modes as well as their occurrence probability under temperature factor,so that effective complement to the traditional FMECA results can be achieved.

Conclusions

The FMECA approach based on ADT presented in this paper fully utilized the advantages of ADT in the fast acquisition of failure samples.So that it is more targeted in identifying the typical failure modes caused by degeneracy failure than traditional FMECA,the failure samples in testability verification test could be supplemented and revised, so that a more adequate and reliable verification of products based on LRM system could be realized.

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