LDPC Anti-Cycle-Slip Analysis and Design for BPSK System

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Abstract: Carrier phase often suddenly change while receiver PLL unlock at PSK modulation communication system, it lead to likelihood information sequence which input of LDPC decoder not accurate and decode fail. This paper analyzed the regularity of LLR information after Cycle-Slip happened and combine with MS decode algorithm improved the Anti-Cycle-Slip decode algorithm. It not only raised the ability of Anti-Cycle-Slip, but also alters the conclusion that all check-nodes degree must be odd number, this found provide a more convenient way for LDPC Anti-Cycle-Slip design.

INTRODUCTION

Some classical methods such as V&V [1] algorithm and PLL loop tracking under the process of carrier recover may cause a problem that phase vague [2]. Carrier phase perhaps change 180° at BPSK system, then the sign of LLR will be become negative. In order to solve that problem usually insert synchronization bites in the data frame, obviously this solution added system burden. Unexpectedly, Anti-Cycle-Slip decode algorithm [3] just added a decode iteration before LLR information input to LDPC decoder, and the problem about phase vague will be overcome easily. The key of algorithm is that by means of look for the relation between check information and variable information, then detected whether system cycle-slip happened or not, after that correct LLR information. But, it demand all of the check-nodes degree in the check matrix are odd number, thus usually need to modify degree distribution function for satisfy the condition. It cause code design more inflexible and decode performance decreased. Moreover, many examples as standard of 802.16e [4] has proposed various LDPC codeword, but not all of the check-nodes degree are odd number. Actually it also can achieve Anti-Cycle-Slip. Another point that original decoding algorithm only depend on single node when judge whether system cycle-slip or not, it likely cause a error judgment. Because of the decoding algorithm has some disadvantage and limitations, this paper made further research and corrected the deficiency, besides proposed a method for LDPC Anti-Cycle-Slip design.

LDPC Anti-Cycle-Slip Decoding Algorithm

Minimum-Sum (MS) Decoding Algorithm

Supposed transmitting terminal information sequence after BPSK modulate is $x(n)$, received information is $y(n)$, through the AWGN channel which mean value is zero, variance is s^2. $v_n, c_m, V(m), C(n)$ respectively represent variable nodes, check nodes, the set of variable nodes and the set of check nodes. At the l^{th} iterative decoding, the belief information transferred by check-nodes c_m to variable nodes v_n is $L^l(\mathrm{r}_{mn})$, the belief information transferred by variable nodes v_n to check nodes is $L^l(q_{nm})$, and the likelihood rate information outputted by variable nodes is L_n^l. The process of MS decoding algorithm [5]:

First：Initialization

$$L_n^0 = \ln\frac{P(x_n = 1 | y_n)}{P(x_n = -1 | y_n)} = \frac{2y_n}{s^2} \quad (1)$$

Calculate the initial likelihood information, and assignment initial value for variable node: $L(q_{nm}) = L_n^0$

Second: Update check nodes

$$L(r_{mn}) = \prod_{n' \in C(n)\backslash n} sign\left[L(q_{nm'})\right] \cdot \min_{n' \in C(n)\backslash n}\left(|L(q_{nm'})|\right) \quad (2)$$

Third: Update variable nodes

$$L(q_{nm}) = L_n^0 + \sum_{m' \in V(m)\backslash m} L(r_{m'n}) \quad (3)$$

Fourth: Iterative termination

$$L_n^k = L_n^0 + \sum_{m \in V(m)} L^k(r_{mn})$$
$$w_n^k = (1 - \mathrm{sgn}(L_n^k)) / 2 \quad (4)$$

Calculate variable nodes information by（4）and make a symbolic decision, if $W_n \cdot H^T = 0$ or reach maximum iteration , Iterative ends.

LDPC Anti-Cycle-Slip Decoding Algorithm

Assume that cycle-slip happened at the starting position of the information sequences, thus we could know that the initial likelihood information shall be opposite after cycle-slip happened from (1). In order to ensure decode correctly, the initial likelihood information must keep unanimous with the non-cycle-slip. If n' is even number, it can ensure that the values of $L(r_{mn})$ invariably in two cases. Thus according to the output of the check information can detect cycle-slip phenomenon by a MS iteration. Specific steps as follows:

（1）Compute the initial likelihood information of variable nodes $L(q_{nm})$;

（2）Calculate the check information $L(r_{mn})$ which the check nodes transfer to the variable nodes for the first iteration according to（2）;

（3）Calculate $T_1(n), T_2(n)$ by（5）;

$$T_1(n) = L_n^0 + \sum_{m \in V(m)} L^1(r_{mn})$$
$$T_2(n) = -L_n^0 + \sum_{m \in V(m)} L^1(r_{mn}) \quad (5)$$

If $|T_1(n)| < |T_2(n)|$, consider as cycle-slip phenomenon has happened. On the contrary, cycle-slip not happened.

Algorithm Improvement

LDPC decode base on MS decoding algorithm, the value of variable-node information will be opposite after cycle-slip compare to not cycle-slip, meanwhile check-node with regularity as follow:

1）while n' is even number, check information invariability after cycle-slip;

2）while n' is odd number, check information shall be opposite after cycle-slip;

when system not cycle-slip, suppose that the sign of check information and LLR are identical (only a few of bit not satisfy this hypothesis).After cycle-slip, if the degree of check-node is odd number, check information and LLR information have same sign, but check-node degree is even number the sign of check information and LLR would be opposite.

$$L_n^1 = L_n^0 + \sum_{m \in V(m)} L^1(r_{mn})$$
$$L_n^1 = L_n^0 + \sum_{m \in V(m)} L^1(r_{mn}) \qquad (6)$$

Make a decoding for variable-nodes, analysis the relation between variable-nodes information and check information, adopt a large number of judgment, it can detect whether cycle-slip or not:

a）Compute variable information L_n^1 and $(L_n^1)'$ for every variable-node.

b）Comparison of value $|L_n^1|$ and $|(L_n^1)'|$ for every variable-node, if the number of variable-node satisfy $|L_n^1| < |(L_n^1)'|$ more than a half, consider as cycle-slip occurred, LLR need to multiply a minus before input decoder, and if the number less than a half LLR information remain unchanged.

Anti-Cycle-Slip Design and Theory Analysis

Suppose that if the number of odd-degree (the degree of node is odd number) check-nodes connect to variable-node more than even-degree check-nodes cycle-slip phenomenon could be detected, contrary not. Then we can compute the detection probability .Compute steps as follow:

Step 1.Compute $p(v_j)$ ($p(v_j)$ is the detect probability of node v_j), q is the proportion of odd-degree check-nodes;

$$p(v_j) = C_{d_{v_j}}^{\frac{d_{v_j}+1}{2}} q^{\frac{d_{v_j}+1}{2}} (1-q)^{\frac{d_{v_j}-1}{2}} + \mathbf{L} + C_{d_{v_j}}^{d_{v_j}} q^{d_{v_j}} \qquad (7)$$

Step 2.Compute the probability of n'（$n' > n/2$）nodes can detect cycle-slip phenomenon. Assume a n dimension vector X , $X = (x_1, x_2, \mathbf{L}, x_j, \mathbf{L}, x_n)$. x_j just has two values 0 and 1, if $x_j = 1$ means that variable-node x_j can detect cycle-slip. $x_j = 1$, $p(x_j) = p(v_j)$; $x_j = 0$, $p(x_j) = 1 - p(v_j)$.

Associated probability distribution:

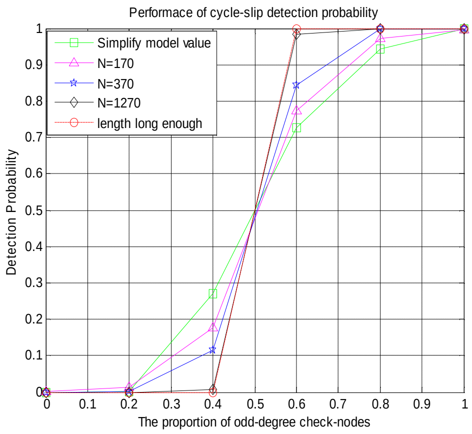
$$P(X) = \sum_{i=1}^{2^n} \left[\prod_{j=1}^{n} p(v_j) \right]_i \qquad (8)$$

$$p(n') = \sum p\left[(X) \,|\, \sum_{j=1}^{n} x_j > \frac{1}{2} n \right] \qquad (9)$$

Some irregular QC-LDPC [6] and not all check-nodes are odd number. variable nodes satisfy mutual independence, figure out the probability of more than a half variable-nodes could detect cycle-slip phenomenon, if value of detection probability is not satisfy, we could modify odd-degree check-nodes proportion or code length.

SIMULATIONS AND DISCUSSION

Parity-check matrix with different proportion of odd-degree check-nodes, simulate the detection probability when cycle-slip has happened. Parameter: AWGN channel, SNR=3dB,simulate times 20000,code length 170, 310 and 1270 ,code rate 1/2 .The results shown in figure 1 and figure 2:



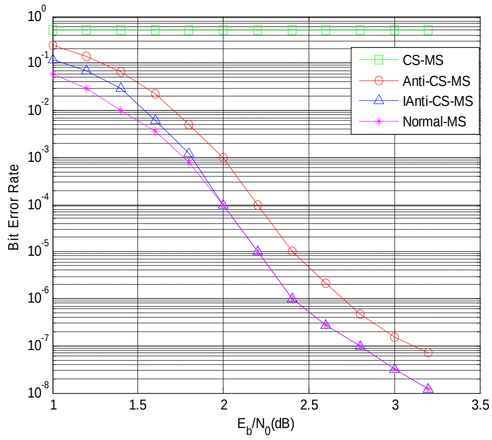


Fig. 1 Performance of cycle-slip detection probability

Fig. 2 The bit error rate

In figure 1 from the curve we found that the ability of detecting cycle-slip phenomenon is raising with the increasing of code length. The theoretical value is derived by limit theorem when the code length is long enough, the result nearly close to code length 1270. Hence, we can make a conclusion that when code length up to a certain extent, just ensure the proportion of odd-degree check-nodes more than a half cycle-slip will be detected accurately.

In figure 2, the codeword is QC-LDCP which code length 1270，code rate 1/2, and the rate of odd-degree to the check-nodes is 4/5.Normal-MS is the performance of MS decoding and cycle-slip does not occurred, IAnti-CS-MS is the error rate curve about improved algorithm when all data frames are cycle-slip. Anti-CS-MS is the error rate curve about original Anti-Cycle-Slip algorithm when cycle-slip occurred, CS-MS is just using MS decoding algorithm meanwhile cycle-slip has happened.

CONCLUSIONS

This paper research of the probability about cycle-slip detection, and proposed a view that needn’t all degree of check-nodes are odd number can also achieve anti-cycle-slip. Other point this paper has given the requirement of anti-cycle-slip when design LDPC codeword. Simulation shows that there three factors may affect the ability of anti-cycle-slip: 1)The proportion of odd-degree check-node; 2) code length ,while length is too short the ability of detecting cycle-slip is not sensitive enough;3) SNR;

In certain range raise the value of proportion, code length and SNR can enhance the ability of anti-cycle-slip, thus need to consider all factors and make a reasonable choose when design for anti-cycle-slip. if select reasonable parameter for LDPC codeword, system can be completely overcome the cycle-slip phenomenon by adopt improved Anti-Cycle-Slip decoding algorithm.

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