Design of a SoC for Intermediate Frequency Digital Receiver

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Abstract. With the development of CMOS technology, the integration and miniaturization have become the trend of electronic devices. This paper proposes a scheme of system on chip (SoC) that realizes the monolithic integration of the intermediate frequency digital receiver based on CMOS technology, which integrates RF receiver front-end, A/D conversion, digital down conversion and baseband processing together. The chip is manufactured by 0.18um CMOS technology, and the area is 7x8mm^2. The test of chip has completed within the RF reception signal range of 0.5~4GHz, The system noise of RF receiving module is below 10dB, the image rejection is greater than 40dB, the SFDR of ADC can reach to 80.22 dB, and the maximum operating frequency of DDC and CPU can arrive up to 100MHz. the test results can meet the requirements of the project evaluation index. The chip has great potential applications in the miniaturization, integration and high reliability of the electronic systems.

Introduction

With the rapid development of modern electronic system integration technology, digital receiver has become the important research content of software radio [1]. Currently, the mature theory and the engineering realization scheme of digital receiver are the intermediate frequency digital receiver. Digital receiver has been widely used in the field of wireless communication, the needs of wireless communication and information services present the explosive growth, the traditional using of discrete devices such as RF front-end, analog-to-digital converter (ADC), digital down converter (DDC) and DSP or FPGA to integrate together as the digital receiver has been unable to satisfy the requirements of the market application for small volume, low cost, low power [2].

With the progress of CMOS technology, the working frequency of single MOS device has risen to microwave, millimeter-wave phase. Therefore, the RF front-end, ADC and digital baseband processing are integrated into a system on-chip (SoC) on a single chip has become possible, compared to the traditional system of circuit board, the SoC of monolithic integrated digital receiver greatly reduces the discrete devices of electronic system, shrinks the volume of the system, improves the reliability of the system.

System Scheme

This paper proposes a novel system scheme, which integrates the RF receiving front-end (RF), analog to digital converter (ADC), digital down conversion (DDC), a microprocessor (CPU) and other digital peripheral IPs into a system on chip (SoC), as shown in Fig.1.The RF receiving front-end adopts the super heterodyne structure, the radio frequency signal received by antenna is transformed to intermediate frequency(IF) through two down-conversions, ADC realizes the sampling and quantization of analog IF signal, the digital IF signal is down-converted to low-frequency digital baseband signal, then decreased the sampling rate into an original sampling rate to facilitate the subsequent signal processing by DDC.

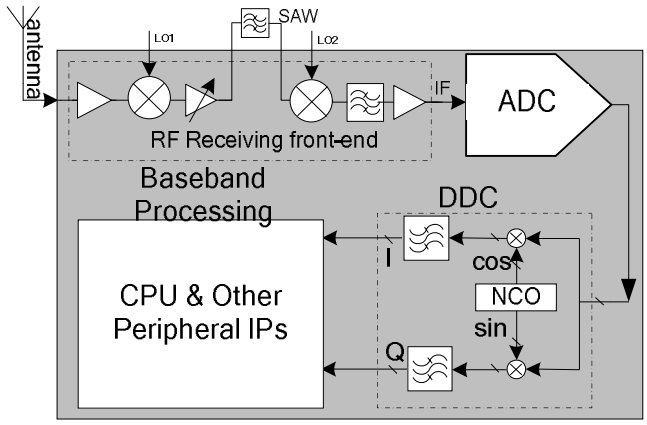

Fig.1 The Proposed System Scheme

Design of Key Modules

A. The Structure of RF Receiving Front-end

The module of RF receiving front-end adopts the super heterodyne scheme, relative to the zero IF architecture, the super heterodyne structure has no DC offset effects, as shown in Fig.2. The module sequentially integrates low noise amplifier (LNA), a mixer (MIXER1), numerical control gain amplifier (PGA), second mixer (MIXER2), low pass filter (LPF), and power amplifier (PA).

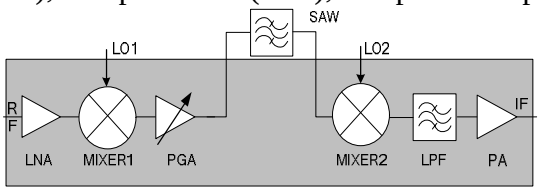

Fig.2 The Structure of RF Receiving Front-end

According to Fig.2, suppose the RF signal received by antenna is $v_{RF}(t)$, whose carrier frequency is ω_{RF} :

$$v_{RF}(t) = V_{RF}\cos(w_{RF}t) \tag{1}$$

The input first local oscillator signal from the outside of the chip is LO_1, whose oscillation frequency is ω_{LO1}:

$$v_{LO1}(t) = V_{LO1}\cos(w_{LO1}t) \tag{2}$$

The signal after the first down conversion is $v_{RF\_LO1}(t)$:

$$v_{RF\_LO1}(t) = \frac{1}{2}V_{RF}V_{LO1}[\cos(w_{RF}+w_{LO1})t + \cos(w_{RF}-w_{LO1})t] \tag{3}$$

The signal after the outside filter (SAW) of the chip filters out the high frequency component is: $v_{RF\_LO1}(t)^*$:

$$v_{RF\_LO1}(t)^* = \frac{1}{2}V_{RF}V_{LO1}\cos(w_{RF}-w_{LO1})t \tag{4}$$

The input second local oscillator signal of the chip is LO_2, whose oscillation frequency is ω_{LO2}:

$$v_{LO2}(t) = V_{LO2}\cos(w_{LO2}t) \tag{5}$$

The signal after the second down conversion is the fellow:

$$v_{RF\_IF}(t)=\frac{1}{2}V_{RF\_LO1}V_{LO2}[\cos(w_{RF\_LO1}+w_{LO2})t+\cos(w_{RF\_LO1}-w_{LO2})t] \tag{6}$$

The output signal of the super heterodyne radio frequency receiving module is obtained:

$$v_{RF\_IF}(t)=AV_{RF\_IF}\cos(w_{RF}-w_{LO1}-w_{LO2})t=AV_{RF\_IF}\cos(w_{IF}t) \tag{7}$$

Eq.7 has the follows: $\omega_{IF}=\omega_{RF\_LO1}-\omega_{LO2}=\omega_{RF}-\omega_{LO1}-\omega_{LO2}$.

B. Structure of A/D converter

Considering the indicator of 14-bit A/D converter (ADC), the ADC employs pipeline architecture. Through the various pipelined sub-level serial connection and parallel work, the pipeline architecture takes into account the chip area and conversion speed, which makes the pipeline technology as the mainstream technology for high-speed, high-precision of ADC. To save power, reduce noise and distortion, the ADC adopts the analog front-end with no pre sample and hold. The structure of ADC is shown as Fig.3, which contains 9-stage pipeline body, internal reference generator, clock circuits, control logic, digital calibration and output driver[3][4]. The 9-stage pipeline who includes a number of multi-stage and each level has multi-bit, disassociates 4 +3 +1.5 x6 +3 respectively, wherein the first stage is the analog front-end protection without sample and hold.

The conventional high-speed pipeline ADC all include the analog front end which is composed of the sampling network and the sample and hold amplifier. Sample and hold amplifier is used to obtain a sample and hold signal for the first-stage pipeline processing. Sample and hold amplifiers tend to consume a lot of power, but also the entire sample and hold amplifier will generate distortion and noise for the ADC. This is because the sample and hold amplifiers are dealing with full swing input signal and no preamp [4].

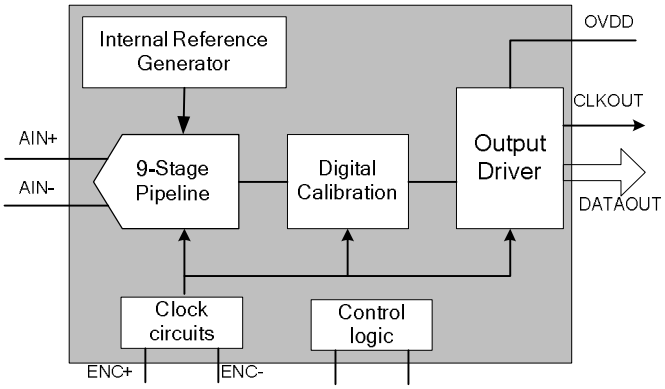

Fig.3 Structure of A/D Converter

C. Design of DDC

Among an all-digital IF receiver, DDC has become a cornerstone technology in wireless communication systems. The main function of DDC is mixing the IF signal from ADC with a digitized cosine for In-phase channel (I-channel) and a digitized sine for the quadrature channel (Q-channel), and down-converting to low-frequency digital baseband signal, then decreasing the sampling rate into an original sampling rate to facilitate the subsequent signal processing. The designed DDC architecture consists of a digital mixer, numerically controlled oscillator (NCO) and digital filter banks. The DDC is divided into I and Q channels, the two data channels share the same NCO unit. The digital filter group was divided into the CIC (cascaded integrator comb) filter module, CIC compensation filter modules and the half-band filter module [5]. DDC block diagram is shown in Fig.4.

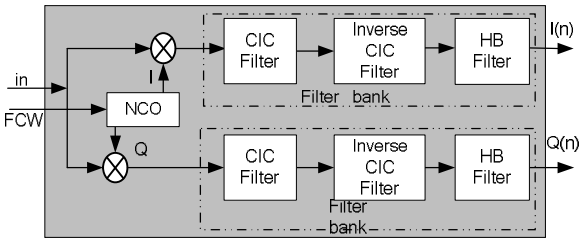

Fig.4 Architecture of DDC

The orthogonal I/Q signal is obtained after filtering the harmonic component in the signal by the low pass filter bank of DDC:

$$\begin{cases} I(n) = \frac{V}{2}\cos[f(n)] \\ Q(n) = \frac{V}{2}\sin[f(n)] \end{cases} \tag{8}$$

Implementation of System on Chip (SoC)

The proposed architecture of Intermediate Frequency (IF) digital receiver SoC shows in Fig.5. The system bus adopts multi-layer bus architecture based on AMBA system, the SoC integrates a processor subsystem, data receiving subsystem, system equipment and peripherals subsystem, and each subsystem connects to the bus through a standard bus interface. The processor subsystem consists of a CPU core, a Serial Flash controller (SflashCTRL), a memory controller (RAMCTRL) and a memory (RAM0). The Serial Flash controller connects the outside Serial Flash chip, which store the system program (such as the operating system). The storage space of RAM0 is designed to 64K Bytes. Data receiving subsystem includes the RF receiving module, A/D conversion unit, digital down conversion (DDC), FIFO, DMA, dual port RAM controller (RAMCTRL1) and RAM1.

The radio frequency signal received by antenna is transformed to intermediate frequency (IF) through twice down-conversion processing of RF receiver module, ADC realizes the sampling and quantization of analog IF signal, the output is down-converted to low-frequency digital baseband signal by DDC, which will be stored in the FIFO, shifted to the RAM1 by the DMA through dual port RAM controller in system. After the CPU issues instructions, data can be read out from the RAM1 through the dual port RAM controller, when the system needs that. To facilitate the signal processing system, the system integrates a 32KB data memory RAM2, as well as UART, GPIO, SPI and TIMERS and other peripherals [5].

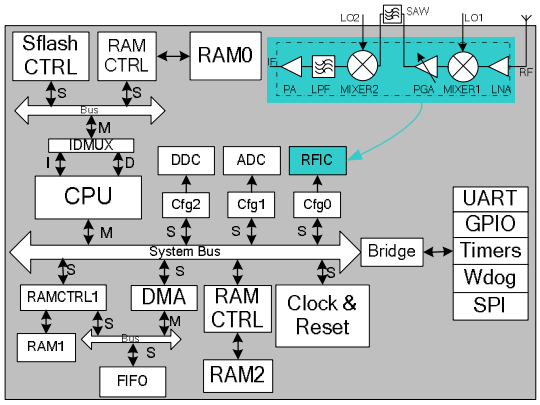

Fig.5 Architecture of If Digital Receiver SoC

Based on 0.18μm CMOS technology, the area of chip is 7x8mm^2 and the number of pad is up to 230, the package of COB is adopted and the chip test system shows in Fig.6, the SoC Chip can receive RF signal between 0.5GHz and 4GHz. The system noise of RF receiving module is below 10dB, and the

image rejection is greater than 40dB. The SFDR of ADC can reach to 80.22 dB, as shown in Fig.7 and the maximum operating frequency of DDC and CPU can arrive up to 100MHz.

Fig.6 The Test System of the Chip

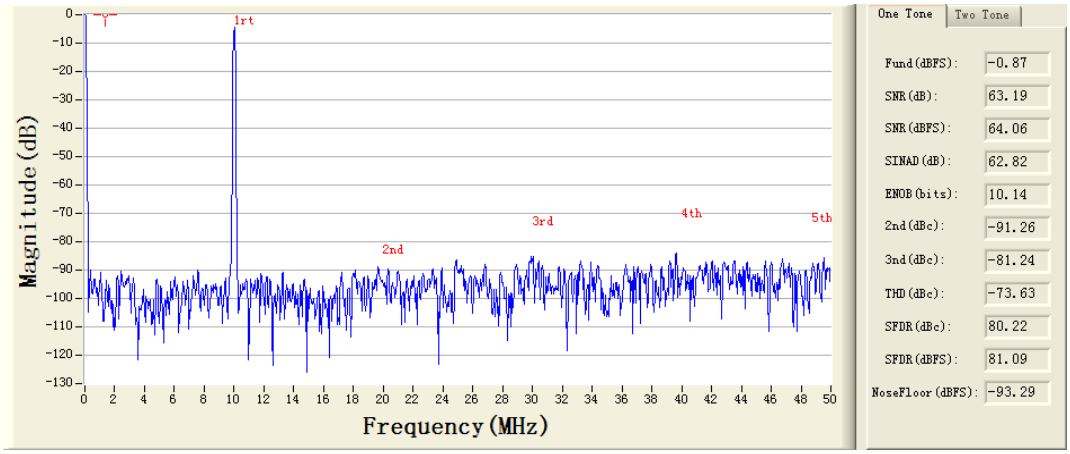

Fig.7 Test Results of ADC Module

Conclusions

This paper has proposed the SoC of intermediate frequency digital receiver based on CMOS technology, which realizes the monolithic integration of RF receiver, A/D conversion, baseband processing. The chip has a great application for the miniaturization, integration and high reliability of electronic system. The chip involves multiple domains of ratio frequency, analog and digital, and faces multiple challenges of designing and technology, the chip has been taped out, and the test results could meet the requirements of the project appraisal index, the next work will be to carry out the optimization of the chip according to the application requirements.

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