

Precise electrical characteristics in light emitting diodes on patterned sapphire substrate

Yang Li^{1, a}, Qiongyong Xing¹

¹ Hainan Technology and Business College, Haikou 570203, China.

^aemail:515832541@qq.com

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Abstract: Accurate electrical properties of semiconductor patterned sapphire substrate light emitting diodes large forward bias voltage were measured by alternating current small signal and I - V plot, as well as our self-built method, respectively. Patterned sapphire substrate light emitting diodes display an obvious negative capacitance at large forward bias which is unexpected and in conflict with Shockley's p-n junction theory that only includes increasing diffusion capacitance and certainly no negative capacitance but in good agreement with conventional sapphire substrate light emitting diodes. The exact relationship between voltage and frequency when negative capacitance appears in patterned sapphire substrate light emitting diodes.

Introduction

High-power light-emitting diodes (LEDs) have received great interest recently due to applications in energy-saving lighting program; therefore the optical and electrical characteristics of LEDs have a significant research value [1-3]. At larger forward bias voltage LEDs display obvious negative capacitance (NC) [4-11]. In daily production, GaN LED epitaxy is on the preparation of the conventional sapphire substrate (CSS) [12,13], the difference of lattice constant between GaN and sapphire substrate material is 14% causing N-GaN epitaxial layer defect density larger and spread to the source area of InGa [14, 15]. Until now, few experiments determining the quantitative relationships between NC and voltage or frequency of patterned sapphire substrate (PSS) LEDs have been reported. This paper use the patterned sapphire substrate (PSS) to prepare the blue light emitting diode which also demonstrated negative capacitance (NC) consist with the results of commercial light-emitting diodes.

In this paper, the capacitance characteristics of PSS GaN light emitting diodes were observed using a measurement method based on alternating current small signal together with direct current I - V plot that were measured by probe station. The precise relation between NC in PSS LEDs and voltage and frequency is obtained. Capacitance increases with the increase of forward bias. Meanwhile, The smaller the frequency, the more obvious the negative capacitance is. These results are in agreement with the predictions of a comprehensive p-n junction theory presented by K. Hess which includes all contributions to the diode current and previous results tested by the group [7-12,17]. By contrast with the results of the experiment and found that in PSS substrate presented is similar to the reported results.

Sample preparation

Growing in the sapphire substrate as dry etching mask layer, mask graphics was produced by lithography process, using ICP etching sapphire substrate and removing the remaining mask layer, and then growing GaN material on it which can urge GaN materials to change from longitudinal extension to lateral extension. This article uses the photoresist etching resistance to replace SiO₂ (or Ni) as a mask, making the ICP etching sapphire on PSS; Photoresist mask could not need to undertake PECVD growth SiO₂, technique or E2Gun steaming metallized, reducing the process steps and improving the production efficiency. The basic structure of PSS is the round hole which is 3 microns in diameter,

spacing of 2 microns and the depth is 864 nm, a hexagonal distribution. MOCVD in PSS production GaN base LED epitaxial films is shown in Fig.1 which is used to the chip manufacturing and testing.

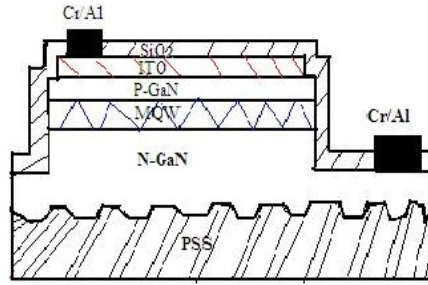


Fig.1: Chip structure of PSS GaN based LED

Measurements

The measuring principles, which were discussed detailedly in previous papers [7-12], are illuminated simply. The equivalent circuit of a real diode and the parallel equivalent circuit used in measurement are shown in Fig. 1(a) and (b), where C and G are the junction capacitance and conductance, r_s is the series resistance, C_p and G_p are the apparent capacitance and conductance, respectively.

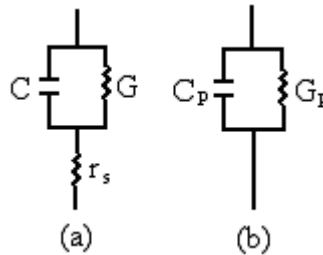


Fig.2. (a) Actual equivalent circuit for a diode;
(b) Parallel measurement circuit.

Comparing Fig.2(a) with (b) we get

$$G_p = \frac{G(1 + r_s G) + r_s (wC)^2}{(1 + r_s G)^2 + (wr_s C)^2}, \quad (1)$$

$$C_p = \frac{C}{(1 + r_s G)^2 + (wr_s C)^2}, \quad (2)$$

At reverse or small forward bias voltages, the junction conductance is often determined by the leaked current. However, at larger forward voltages, it is displayed mainly by the differential conductance which is often larger than the DC conductance. At large forward bias, $G \gg wC$ is held, equations (1) and (2), therefore, can be simplified to

$$r_s = \frac{1}{G_p} - \frac{1}{G}, \quad (3)$$

$$C = (1 + r_s G)^2 G_p, \quad (4)$$

The $I - V$ characteristic of diodes is

$$I = I_s \left(e^{\frac{qV_j}{nkT}} - 1 \right), \quad (5)$$

where the junction voltage is given by $V_j = V - r_s I$. When $V_j \gg nkT/q$ the junction conductance G consists mainly of differential conductance and is given by

$$G = \frac{dI}{dV_j} = \frac{qI}{nkT} \left(1 - \frac{V_j}{n} \cdot \frac{dn}{dV_j} \right) \quad (6)$$

Thus, one can accurately determine the dependences of junction parameters of LEDs on the forward bias voltages by combining Eqs (3)-(6).

Using above method we measured a plenty of LEDs. All measured LEDs display obviously NC at large forward voltages, here, we measured two blue LED manufactured by PSS named 1# and 2# respectively.

In our measurements, the I - V curves、apparent conductance G_p and apparent capacitance C_p were measured by probe station which is used to physically acquire signals from the internal nodes of a semiconductor device. All measurements were performed at room temperature.

Results and discussion

Fig. 3 shows the relationship between current and forward bias voltage of samples. In the inset, the $\ln I$ - V curves are clearly divided into two linear sections. In fig.3, we can observe that the current increases rapidly with the increasing of voltage from 2.7V to 3V, besides, the logarithmic curve is nearly linear when the voltage is greater than 3V. Because of slope= $qV/(nkT)$, the change of slope implies that the ideality factor n is the voltage dependence and increases a little with the increasing voltage. The slope is about 5.8 at the corresponding range of voltage from 6 to 10V, then n obtained from slope is about 6.6, which is larger than the classical theoretical value of 2 and previous experiments [8-10]. This relatively small slope is mainly influenced by the series resistance and thereby will be dependent on the current crowding effect.

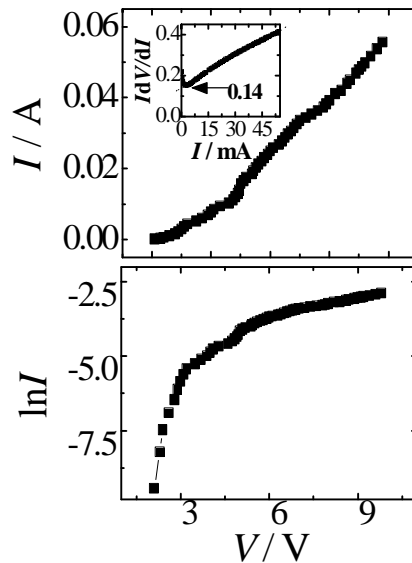


Fig.3 I - V and $\ln I$ - V plots of LEDs

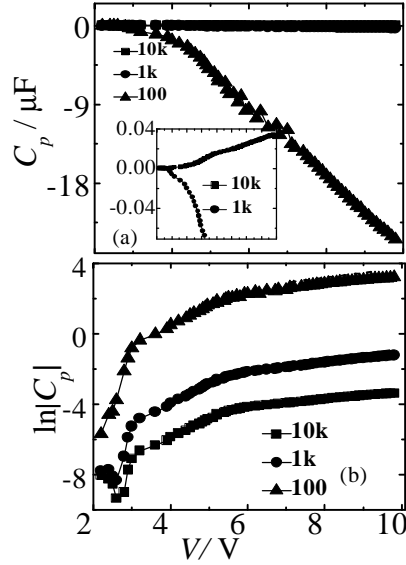


Fig.4 (a) Dependences of apparent capacitance C_p of 1# sample on forward bias voltages .
 (b) The curves of the absolute values of capacitance on voltages

Fig.4 shows the forward $C_p - V$ profiles for 1# sample at 100, 1 k and 10 kHz. In insert graph of (a), it tells us that with the forward bias voltages increasing, the terminal capacitance increases firstly to a positive maximum and then becomes negative. The NC effect is more noticeable at lower frequencies and higher forward bias voltages, which is in good agreement with the NC behavior reported obviously [7-12]. It can be seen that what a different when the voltage is greater than 7V, capacitance began to have significant decline. In previous reported, when negative capacitance appeared, the forward bias was far less than 7V. This illustrates that patterned sapphire substrate LED can withstand the greater voltage. In fig.4, at large bias the $\ln|C_p| - V$ profiles for the PSS LED at different frequencies are parallel, and $\ln|C_p|$ increases linearly with voltages showing in fig.4, i.e. $|C_p| \propto e^{mV}$. Fitting $\ln|C_p| - V$ plots, the slope of fitting linear is about 4, namely $m \approx 3.9$. From theoretical point of view, the relation of conductor or capacitance with voltage is G_p or $|C_p| \propto e^{qV_j/nkT}$, where q is the electron charge, n the ideality factor, k Boltzmann's constant, T temperature, and V_j the voltage across the junction. At room temperature, $kT \approx 0.0259qV$, using $m \approx 3.9$ one can get the ideality factor of 1# is about 9.8, which is far larger than the classical theoretic value 2 and experimental results [8], but it is so close to the ideality factor n from fig.3. But in fact, we have to point out: 1) the ideality factor discussed in this work is not a conventional factor, because it includes the effects of encapsulation and contact of measurement electrode-poles, as well as other factors of measurement and instrument; 2) excepting these external factors, the internal structure of p-n junction can also lead to a large ideality factor. For example, the influence of additional rectifying heterojunctions and metal-semiconductor junctions of diodes [14-16]. Besides, our samples are produced by PSS. All above conditions make a larger ideality factor.

In order to affirming quantitative relation between capacitance and forward bias and frequency, we draw a Fig.5 which is shown in following. In fig.5(a), at different voltages, NC is obvious at low frequency. Fig.5(b) shows the $\ln|C_p| - \ln f$ plots, it can be seen that at large forward bias, $\ln|C_p|$ nearly decreases linearly with frequencies increasing, for sample 1, when the value of voltage is 4.5V, the

insert graph shows that the plots of $\ln|C_p| - \ln f$ has no regularity. Perhaps the reason is that when the voltage is lower, NC phenomenon is not noticeable and distracted in the test. The slopes of $\ln|C_p| - \ln f$ curves are about 1.02. So we can conclusion that the absolute values of NC nearly increase more than one magnitude when frequency decreases a magnitude. The precise relation between NC and frequency is, $C_p = f^{-b}$, where b is corresponding to the slopes of $\ln|C_p| - \ln f$. Obviously, the value of b is different with disparate materials. Synthesize the conclusions of Fig.4 and Fig.5, one gets $C_p = -C_0 f^{-b} e^{mV}$. ($1 < b < 2$)

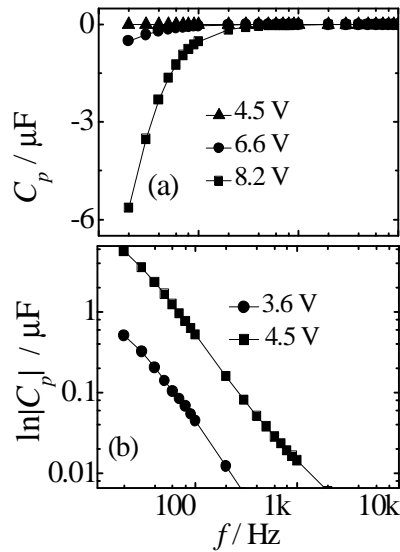


Fig.5 (a) Dependences of apparent capacitance C_p of 1# sample on frequency. (b) The curves of $\ln|C_p| - \ln|f|$.

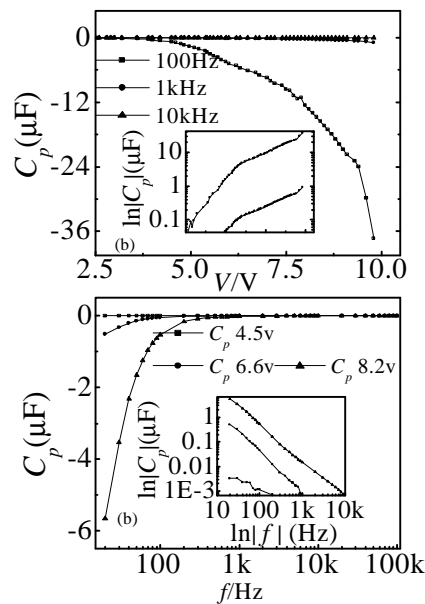


Fig.6 (a) Dependences of apparent capacitance C_p of 2# sample on forward bias voltages (b) Dependences of apparent capacitance C_p of 2# sample on frequency. The insert graph is the curves of $\ln|C_p| - \ln|f|$

Same results were obtained for 2# sample as shown in fig.6. From the relation between NC and voltage and frequency, one can conclude that the dependence of NC on voltage and frequency of PSS LEDs is

$$C_p = -C_0 f^{-b} e^{mV} \quad (1 < b < 2) \quad (7)$$

Where C_0 is a constant for a given LED. The equation (8) was derived in [7-9], and it was suitable for PSS LEDs.

In this work, the forward dielectric characteristics of LEDs prepared by GaN-based LEDs on patterned sapphire substrate were measured accurately with ac small-signal and I-V. Apparent properties which were similar to CSS LEDs used HP4285A LCR meter and a TH2819 precision LCR meter were measured by probe station. Experimental data indicate that the NC in PSS LEDs grows exponentially with applied bias voltage, which is unexpected because it is in conflict with Shockley's p-n junction theory which only includes increasing diffusion capacitance and certainly no NC. Furthermore, negative terminal capacitance confirms the prediction of Laux and Hess' theory [14]. In addition, the quantitative relation between NC and frequency of PSS LED is obtained. From the slopes of semi-logarithmic curves of currents, $a|C|$ on voltages and frequency, the precise quantitative description of G_p and C_p is obtained $C_p = -C_0 f^{-b} e^{mV}$. Meanwhile, PSS LEDs can withstand the greater voltage [12].

Acknowledgements

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