

Design of Frequency Characteristic Test Instrument Based on USB

Zhengling Wu¹, Nannan Zhang²

¹College of information and control engineering, Jilin Institute of Chemical Technology, Jilin, Jilin 132022, P.R. China.

²China people's Liberation Army Reserve Division forty-seventh, Jilin, Jilin 132013, P.R. China.

Keywords: Frequency characteristic, Test instrument, USB, Design.

Abstract: Aiming at the issues of high cost, large size, high maintenance cost for traditional frequency characteristic test instrument, this paper introduces a design process of frequency characteristic test instrument based on USB2.0. The whole system took single clip microcomputer as the control core, and the sweep signal was produced by frequency synthesizer AD9850, so as to realize the measurement of network frequency characteristic. The measured data is transmitted via USB to PC for display, storage and playback. Finally, the feasibility and accuracy of scheme were verified through the experimental tests.

Introduction

In the electronic measurement, the amplitude frequency characteristic and phase frequency characteristic of the network often need to be measured, and the instrument that is used to realize the above measurement is frequency characteristic test instrument^[1-2]. At present, it can be broadly divided into two categories: one is the traditional equipment, such as domestic BT type low frequency characteristic tester, which is difficult to meet the needs of users, especially in the field of automatic testing requirements, due to the disadvantages of the heavy equipment, large volume, complicated operation, etc.; another is tester fabricated by large-scale new type chip technology, which has the advantages of excellent performance, high precision and so on, but it is generally imported products, expensive, difficult to maintain^[2-4]. Therefore, this paper introduces a frequency characteristic test instrument based on USB. It does not only has the advantages such as low cost, small volume and convenient operation, but it can also make full use of the computer resources, so as to the analysis, storage and display of test results.

System general structure

The overall structure block diagram of system is shown in Figure 1, which consists of two parts: hardware and software. The hardware part is composed of test hardware circuit, USB interface, PC; the software part is composed of firmware software layer, driver layer software and client application layer software.

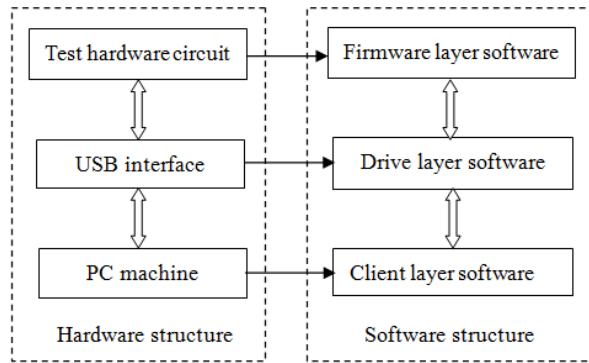


Figure 1 Overall structure diagram of the system

System hardware circuit design

The hardware structure of the system is shown in Figure 2, according to the function which is divided into: signal generation, conditioning circuit, detection circuit and control communication circuit. Test instrument generates sweep signal through single chip microcomputer AT89S52 controlling DDS (direct digital synthesis) frequency synthesizer AD9850^[5-6]. The amplitude frequency characteristic and phase frequency characteristic of tested network are realized by the A/D circuit, and then sent to the upper computer through the USB interface.

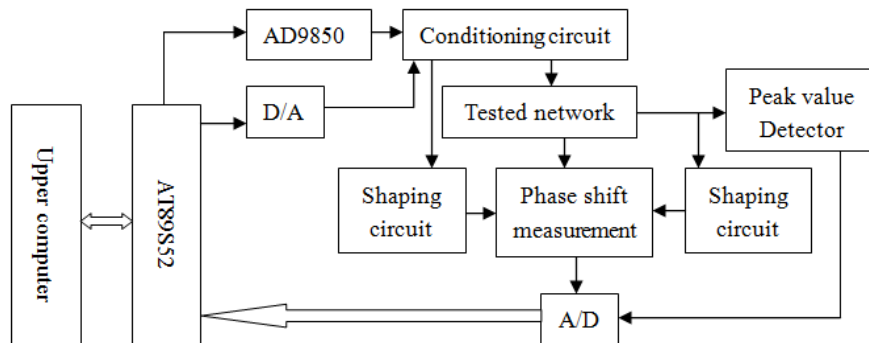


Figure 2 Hardware structure diagram of system

When the sweep frequency mode output signal, the single microcontroller convert the received frequency control word into starting frequency and cut-off frequency, and the sweep frequency step is calculated according to the sampling points required by the system, in order to output the sweep frequency signal source with the step sending frequency control word to DDS. The obtained sweep frequency signal has stable amplitude in the sweep frequency range through the signal conditioning circuit. Signal conditioning is sent to tested network for the amplitude measurement and phase comparison, and then the analog signal amplitude and phase difference signal were converted to digital quantity and sent to MCU processing after A/D sampling, finally the single microcontroller transmit the processed results to the upper computer. According to the results the upper software draws out the curve diagram of amplitude frequency characteristic and phase frequency characteristic for the measured network.

Sweep frequency signal design

The clock using in the design is 20MHZ, the word length is 32 bits, and the minimum output frequency, i.e. frequency resolution is:

$$f_L = f_{clk} / 2^{32} = 20 \times 10^6 / 2^{32} \approx 0.0047 H_z$$

When the output maximum frequency is about 1/4 of the clock frequency, the maximum output frequency is:

$$f_M = f_{clk} / 4 = 5MHz$$

Setting K is the frequency control word for DDS, according to:

$$f_{out} = K \times f_{clk} / 2^{32} = K \times 20 \times 10^6 / 2^{32} \quad (1)$$

It can be concluded that the frequency control word of DDS is:

$$K = f_{out} \times 2^{32} / 20 \times 10^6$$

According to the need frequency of output signal, the output frequency control word K is calculated and converted integer by formula (1), which is sent to AT89S52 through the USB interface and sent into FREQ0 or FREQ1 of AD9850 through the serial, so as to output the needed signal. The sweep frequency signal is generated with the change of frequency control word K.

Signal conditioning circuit design

Figure 3 shows the circuit in which the sweep frequency signal output by DDS amplifies or attenuates programmable, to a certain extent, it also plays a filter effect. When the DDS output current setting resistor R17 is 3.9KΩ, output resistance R3, R4 are 50Ω, output voltage $V_{P-P} \approx 200mV$. Circuit used 8-bit D/A is divided into 256 gear control output voltage amplitude, and the gain range of AD603 is -11dB to 30dB in the frequency range 90mhz, so the minimum output amplitude of AD603 is $V_{P-P}=60mV$. The maximum output voltage is limited by the AD converter reference voltage, so the peak only reach the reference voltage, in order to improve the load capacity and joined a level follow.

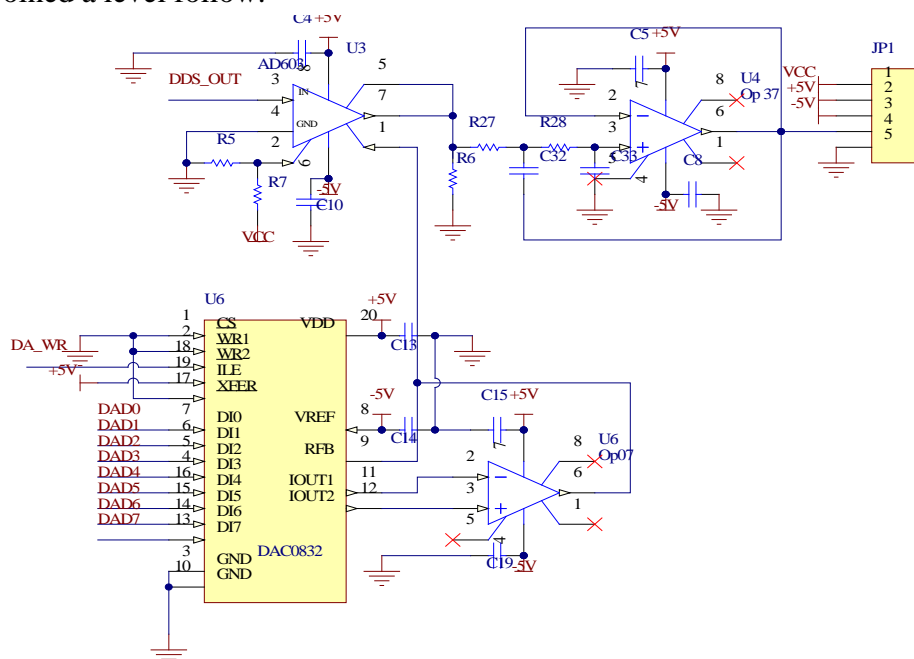


Figure 3 Circuits of signal conditioning and amplitude regulation

Circuit design of signal detection

The detection circuit is divided into phase frequency detection circuit and amplitude detection circuit. Amplitude detection use peak detector and the detection circuit adopt the DC compensation circuit so as to effectively suppress the diode voltage drop, to compensate the bias voltage of 0.7V,

and the circuit is shown in Figure 4. The input and output peak signals for measured network are detected using active peak detector, sending to an A/D converter to fulfill the quantization.

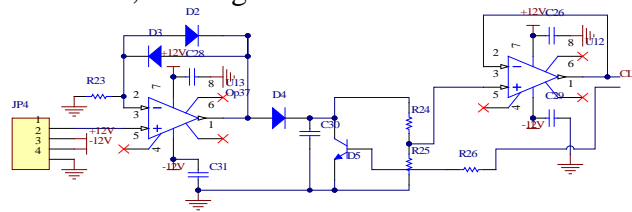


Figure 4 Detector of active peak value

Figure 5 shows the circuit for phase difference measurement circuit. The main value range of phase difference is -180° to $+180^\circ$. The input and output signals of the measured network are transformed into rectangular wave through the shaping circuit, and the signal is sent into the phase difference measurement circuit. Two groups outputs of LM393 in Figure 5 are the rectangular waves obtained by the input and output signals of the measured network. The P3.7 port sent from output of D trigger to the single clip microcomputer is the basis to judge the lead or lag. If it is in high level, "+" is added before the phase difference φ , on the other hand, add "-". φ is sectionally measured due to the frequency range of the measured signal is wide.

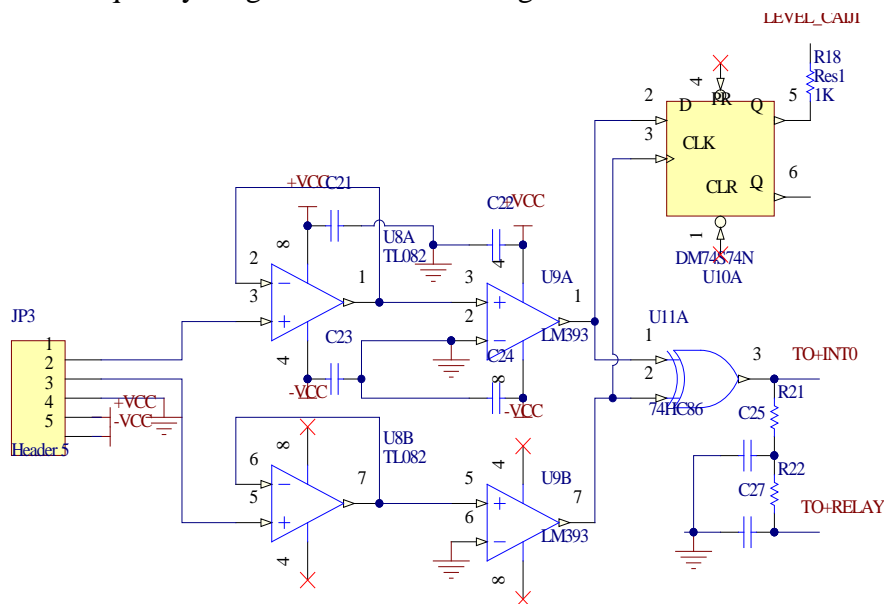


Figure 5 Phase difference measurement circuit

Design of system software

Software flow chart

The system selects the AT89S52 single clip microcomputer to mainly complete the communication with PC, control DDS to generate sweep frequency signal and process the sweep frequency signal output amplitude using the program control, and the software flow chart is shown in Figure 6.

Note: the highest setting frequency range is 1Hz-999.999KHz; the lowest sweep frequency signal output amplitude $V_{P-P}=60\text{mV}$; the highest sweep frequency signal output amplitude $V_{P-P}=5\text{V}$; the fixed sampling quantity is 10000 points.

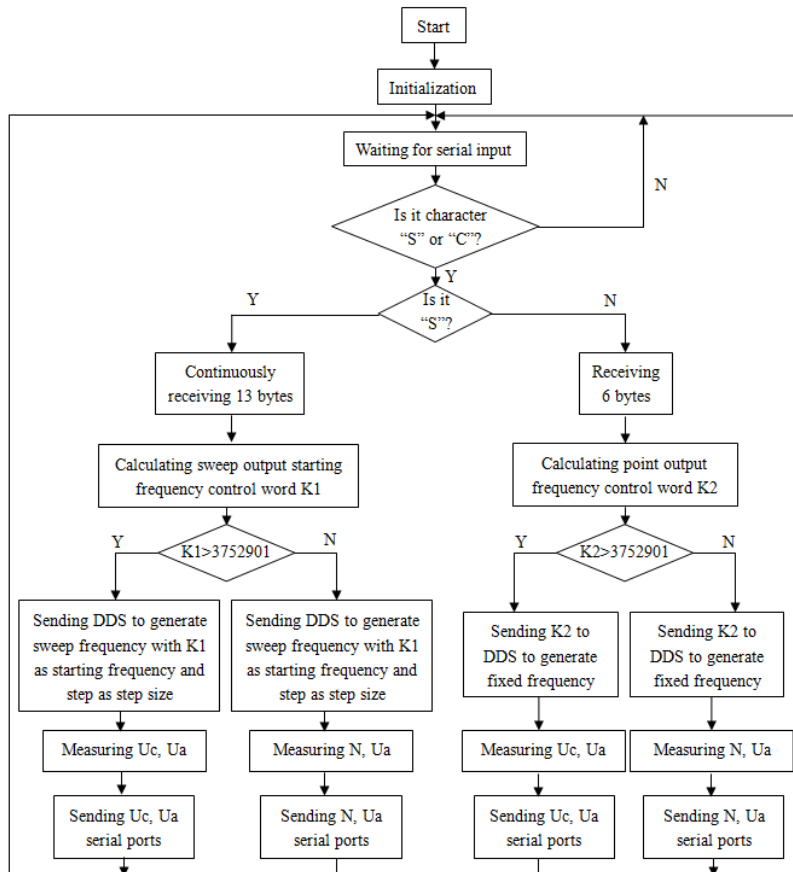


Figure 6 Software flow chart

Correlation calculation and algorithm

1) Phase calculation

The formula is:

$$N_f = \phi \times 2^{14} / 2\pi \quad (2)$$

where N_f is the corresponding phase control word, ϕ is the phase deviation. For example: when calculating 15° phase, there are:

$$N_f = (\pi/12) \times 2^{14} / (2\pi) = 682(D) = 2AA(H)$$

The initial phase of the DDS output can be 90 degrees using the phase setting, which is convenient for reducing the time of the peak detector reaching peak, thus reducing the measurement error.

2) Frequency calculation

To AD9850, the formula of 32 bit frequency control word is:

$$N = 2^{32} \times f_o / f_r \quad (3)$$

where f_r is the reference clock source frequency, f_o is the output frequency. The set output frequency f_o is 6 digit decimal number: $a_0 a_1 a_2 a_3 a_4 a_5$, the order is from high to low, if $a_0 = 1$, $a_1 \sim a_4$ are all 0, $f_o = 0.999999MHz$. The longest length of integer arithmetic supported by C language compiler is 32 bit (long type), so the method combined look-up table and calculation

is used in program when calculating 32-bit frequency control word. Let n_0 , n_1 and n_2 be the frequency control word corresponding to 1MHz, 1kHz and 0.1Hz, respectively.

Setting intermediate variable b_0 , b_1 and b_2 , make:

$$b_0 = a_0 \times 10 + a_1, \text{ unit is MHz};$$

$$b_1 = (a_2 \times 10 + a_3) \times 10 + a_4, \text{ unit is kHz};$$

$$b_2 = [(a_5 \times 10 + a_6) \times 10 + a_7] \times 10 + a_8, \text{ unit is 0.1Hz};$$

$$N = b_0 \times n_0 + b_1 \times n_1 + b_2 \times n_2$$

Because $n_0 > 2^{32}$, $n_2 \leq 2^{32}$ and $n_1 \leq 2^{32}$, $b_0 \times n_0$ in program is derived directly by looking-up the table and $b_1 \times n_1$ is obtained by calculation; n_1 , n_2 can be divided into low 16 bits and high 16 bits to calculate respectively, and the low 16 bits results carry (i.e. the part exceed 16 bits) need to be added into the high 16 bits results. The intermediate variables f_0 and f_1 can be set, and the low 16 bits of each calculation results is placed in f_1 , high 32 bits is placed in f_0 (f_0 and f_1 are 32 bit word length). The method combined look-up table with the calculation is simpler and faster in calculation compared with the direct calculation method.

For AD9850, 1MHz, 1kHz and 0.1Hz correspond to 40 digit numbers n_0 , n_1 and n_2 :

$$n_0 = 2814749767106(\text{D}) = 28\text{F}5\text{C}28\text{F}5\text{C}2(\text{H});$$

$$n_1 = 2814749767(\text{D}) = \text{A}7\text{C}5\text{AC}47(\text{H});$$

$$n_2 = 281475(\text{D}) = 44\text{B}83(\text{H});$$

Measured results and analysis

Measured results

Table 1 Output frequency and amplitude test data (there is no stable amplitude)

Test item	Measured data		
	Setting frequency	Tested frequency	Output amplitude (V_{P-P})
Sine Wave Output	100Hz	100.01Hz	0.2
	500Hz	500.0006Hz	0.2
	1000Hz	1000.0061Hz	0.19
	5000Hz	5000.0086Hz	0.17
	10000Hz	10000.0582Hz	0.18
	50000Hz	50000.0889Hz	0.17
	200000Hz	200000.1450Hz	0.17
	999999Hz	999.9990kHz	0.14

Table 2 Output amplitude tested data (output amplitude can be adjusted manually)

Test item	Output frequency	Output amplitude (V _{P-P})
After a stable band with load	50 Hz	1
	1000 Hz	1
	10000 Hz	1
	100000 Hz	1

The output frequency is tested using the frequency meter, the output waveform test data observed by the oscilloscope are shown in Table 1 and Table 2, which display that the designed DDS output frequency is: 1Hz ~ 999999Hz, frequency step is: 0.1Hz.

Low pass frequency response test

The RC low pass network is measured using the designed frequency characteristic tester, and the actual measured amplitude frequency characteristic is shown in Figure 7.

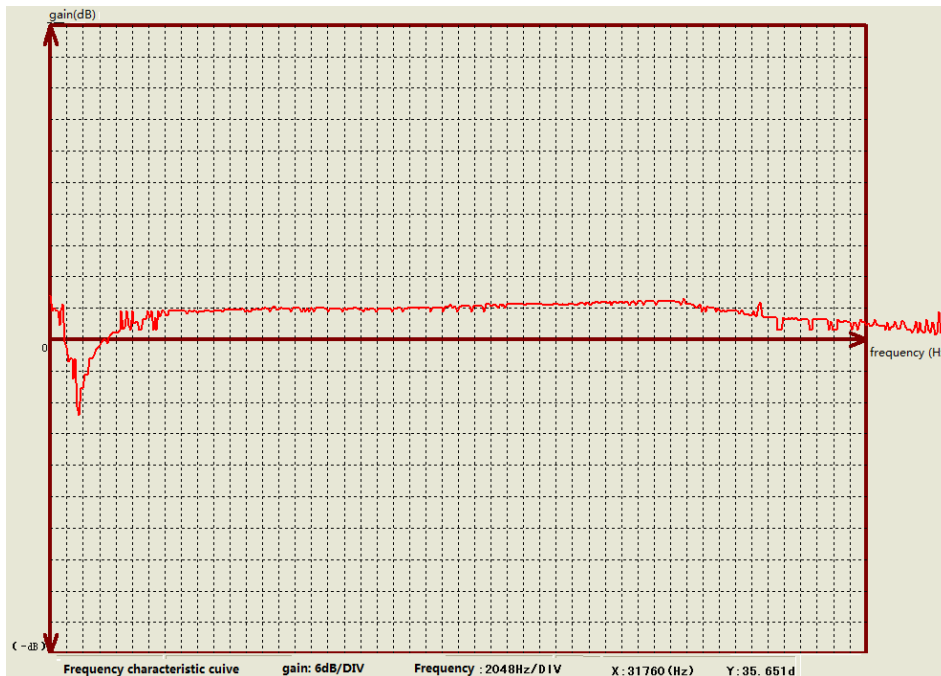


Figure 7 Amplitude frequency curve

Note: R=10k, C=4700PF; the abscissa is the frequency (Hz), the ordinate is the gain (-dB)

Figure 8 shows the results for EWB simulation of the same parameter, through contrast it can be seen the theory and the actual curve is basically the same.

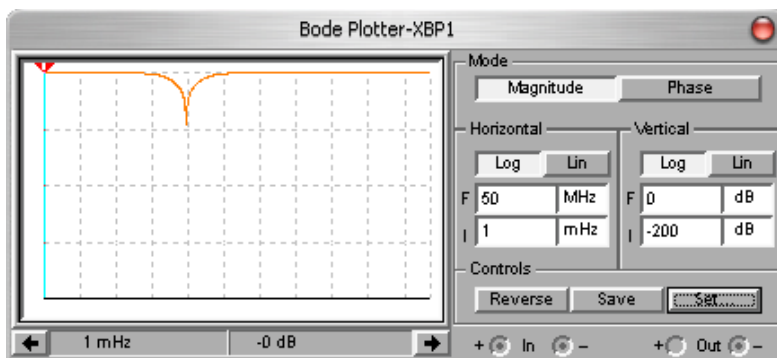


Figure 8 Amplitude frequency curve of EWB simulation (unchanged parameters)

Conclusions

This paper introduces a frequency characteristic test instrument based on USB and the system sweep frequency signal is produced using the DDS integrated circuit AD9850. The actual minimum stepping is 0.1Hz under 20 MHz clock. The sweep frequency signal quality is higher, and sweep frequency range is wider, and then it can be more accurately to measure the frequency characteristics of tested network. After many experiments, it shows that the frequency characteristic curve of the system is consistent with the theory, and the performance is stable and reliable. The frequency characteristic test instrument has the advantages of small size, convenient operation and reliable performance. It can be a good assistant instrument for scientific research, teaching and experiment.

References

- [1] Yanhua Yang. Design and implementation of low cost frequency characteristic testing instrument [D]. Taiyuan: Taiyuan University of Technology, 2005. (in Chinese)
- [2] Ruifen He. Design of sweep frequency instrument based on DDS technology [D]. Lanzhou: Northwest Normal University, 2013. (in Chinese)
- [3] Song Chen, Jun Rong. Design of a simple digital control frequency characteristic testing instrument [J]. Electronic Device, 2015, 38(4):868-875. (in Chinese)
- [4] Jing Lu, Zhiou Xu. Design of sweep frequency signal source based on DDS chip [J]. Coal Mining Machinery, 2006, 8:18-20. (in Chinese)
- [5] Xilin Chai, Manhong Fan, Weizhao Zhang, Jinlong Li. Design of a simple portable frequency scanning instrument based on DDS [J]. Automation and Instrumentation, 2014, 8:41-43. (in Chinese)
- [6] Weibo Cong, Yong Yang, Qingkai Han. USB interface design of low power data acquisition system [J]. Application of single chip microcomputer and embedded system, 2005, 1:25-27. (in Chinese)