Software Phase Locked Loop for Single Phase Grid Tied Systems

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Abstract. The phase angle utility is a critical piece of information for operation of power devices feeding power into the grid like PV inverter.A Phase Locked Loop (PLL) is a closed loop system in which an internal oscillator is controlled to keep the time/phase of an external periodical signal using a feedback loop.In this paper,a method is proposed to enhance the performance of a phase locked loop.An adaptive notch filter is used to selectively notch the exact frequency.Simulation of both the basic PLL and the improved PLL are made by MATLAB/Simulink,the result is summarized in the last section.

Introduction

The PLL is simply a servo system which controls the phase of its output signal such that the phase error between the output phase and the reference phase is minimum.The quality of the lock directly effects the performance of the control loop of grid tied applications.As line notching, voltage unbalance,line dips,phase loss and frequency variations are common conditions faced by equipment interfacing with electric utility the PLL needs to be able to reject these sources of error and maintain a clean phase lock to the grid voltage.

The principle of phase locked loop

With the development of digital signal processor,PLL is more likely to be implemented by software.Fig.1 shows the block diagram of a basic software phase locked loop,which consists of a phase detector (PD),a loop filter (LF) and a voltage controlled oscillator (VCO).

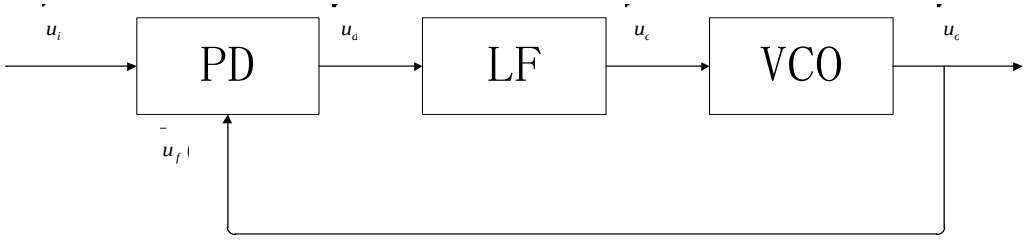

Fig.1 Phase Lock Loop Basic Structure

In order to explain this principle more vividly,a measured value of the grid voltage is given by,

$$u_i(t) = U_i \sin(\omega_i t + \theta_i) \tag{1}$$

And the out put of the PLL is,

$$u_o(t) = \cos(\omega_o t + \theta_o) \tag{2}$$

Now we get both the phase of input and output,the phase detector is built to get the difference between input phase and output phase,since

$$\sin\alpha * \cos\beta = \frac{1}{2}[\sin(\alpha+\beta) + \sin(\alpha-\beta)] \tag{3}$$

The phase detector multiplies the measured value and the output value to get,

$$u_d(t) = \frac{U_i}{2}\{\sin[(\omega_i+\omega_o)t + (\theta_i+\theta_o)] + \sin[(\omega_i-\omega_o)t + (\theta_i-\theta_o)]\} \tag{4}$$

Eq.4 shows that the output of phase detector has information of the phase difference.However it has a high frequency component as well.

The block followed by PD is a low pass filter,with this block,the high frequency components is filtered.In this particular case,the output of LPF is

$$u_c(t) = \frac{U_i}{2}\sin[(\omega_i - \omega_o)t + (\theta_i - \theta_o)] \tag{5}$$

So far,we have been processing voltage signals,but the PLL is built to get the phase of the grid,so we need the last block to turn the voltage signal into the phase signal.

The voltage controlled oscillator turns the the voltage signal into the phase signal,hence

$$\omega_c(t) = f[u_c(t)] \tag{6}$$

If the difference of angular frequency between the grid and the output of VCO is zero,recording to Eq.5 ,the out put of LF is a constant,and considering that the sample time of the software PLL could be very short,the relationship between voltage and phase is linear.So we can rewrite Eq.6

$$\omega_c(t) = \omega_f + Ku_c(t) \tag{7}$$

With a integrator,we can transform the angular frequency into instantaneous phase

$$\theta_c(t) = \int_0^t \omega_c(t)dt = \omega_f t + K\int_0^t u_c(t)dt \tag{8}$$

Adaptive notch filter

The LF is a low pass filter,the parameters of LF directly affects the performance of PLL.But the condition for PLL for grid tied systems is critical,the frequency of the grid is very low (50Hz).The roll off provided by the LPF is not good enough.

In this case,a notch filter is introduced to the loop.Eq.4 shows that the output of PD contains the twice the grid frequency component,the notch filter should be able to selectively notch the exact frequency which shows in Eq.4.

A typical transfer function for a notch filter is

$$H(s) = \frac{s^2 + 2\zeta_2\omega_n s + \omega_n^2}{s^2 + 2\zeta_1\omega_n s + \omega_n^2} where \zeta_2 << \zeta_1 \tag{9}$$

Since $\zeta_2 << \zeta_1$,we set ζ_2=0.00001 and ζ_1=0.1,then we take China in which the grid frequency is 50Hz,now we can get the response of the notch.The Bode diagram shows in Fig.2

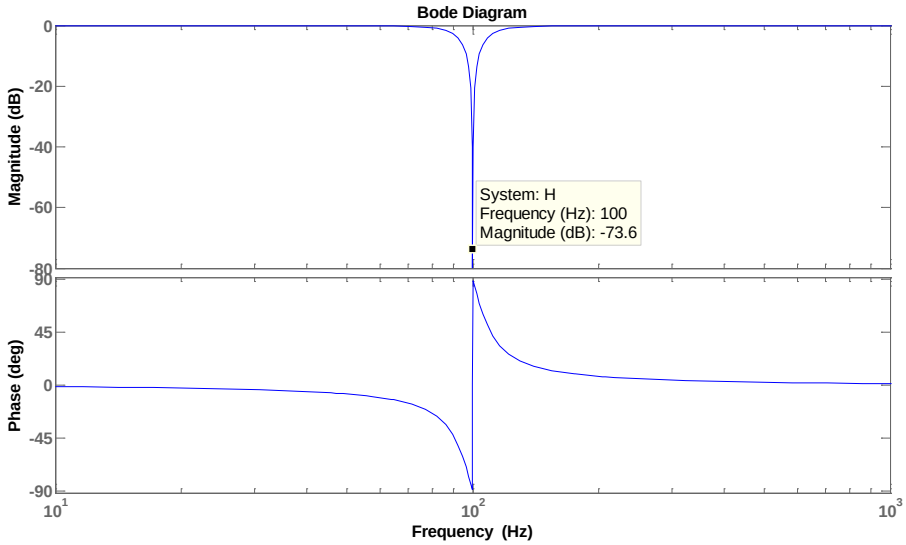

Fig.2 Bode diagram of notch filter

Fig.2 shows that the notch filter roll off the exact component at twice the grid frequency.So we attach this notch filter to the PD,the output voltage of PD ($u_d(t)$) go through notch filter and get

itself filtered,in this case the design of LF can focus on the LPF characteristics without worrying about the twice grid frequency component.So the structure in Fig.1 may redraw as Fig.3 below,

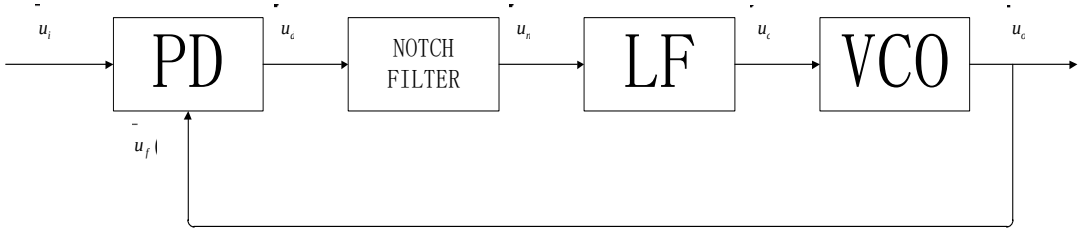

Fig.3 PLL wit a notch filter

Since it is about software PLL,we should transform the transfer function from s domain into z domain.

Using zero order hold $s = \frac{z-1}{T}$,Eq.9 turns into

$$H(z) = \frac{z^2 + (2\zeta_2\omega_n T - 2)z + (-2\zeta_2\omega_n T + \omega_n^2 T^2 + 1)}{z^2 + (2\zeta_1\omega_n T - 2)z + (-2\zeta_1\omega_n T + \omega_n^2 T^2 + 1)} = \frac{B_0 z^2 + B_1 z + B_2}{A_0 z^2 + A_1 z + A_2} \tag{10}$$

Here T means the sample time.

More specific,

$$u_n(n) = -A_1 u_n(n-1) - A_2 u_n(n-2) + B_0 u_d(n) + B_1 u_d(n-1) + B_2 u_d(n-2) \tag{11}$$

Here n means current sampling time,n-1 means last sampling time.

Simulation

The system above is simulated in MATLAB/Simulink.The effective value of the grid voltage is given by 22V,the grid frequency is 50Hz and the frequency of calling the PLL routine is 20kHz.

The waveform of grid voltage and the phase calculated by a basic PLL without notch filter are shown in Fig.4

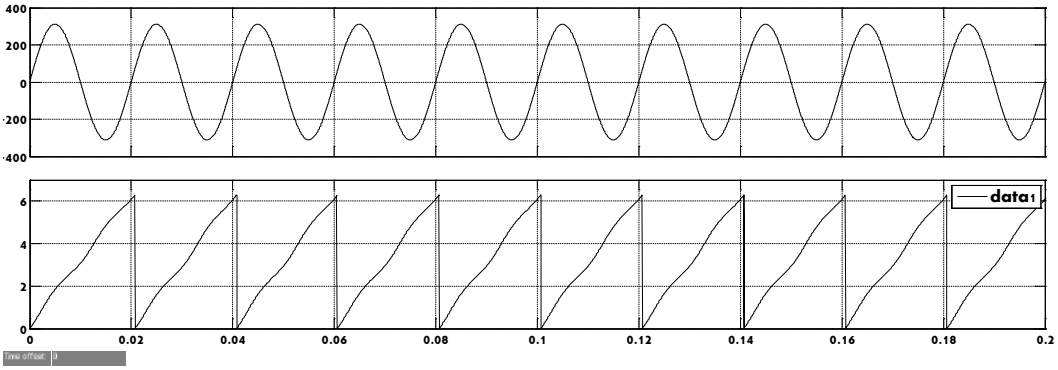

Fig.4 The out put of PLL without notch filter

In order to illustrate the effect of the notch filter,the phase calculated by a PLL with notch filter is added to Fig.4 as shown in Fig.5.

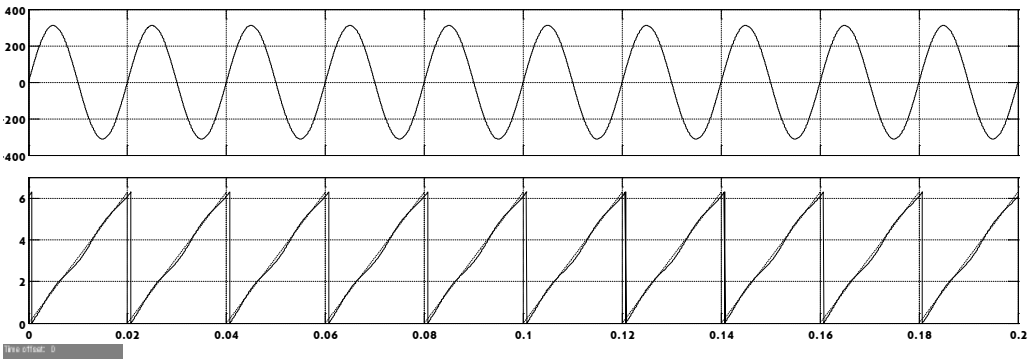

Fig.5 The out put of PLL with notch filter

Summary

The dashed line shows the output of a PLL with notch filter.With the same LF,the dashed line is closer to the right phase illustrated by the grid.According to Fig.5,the notch filter can help the PLL to lock the phase more precisely.

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