The research and design of 5.8GHz RF front-end receiver based on double balanced resistive mixer

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Key words：Double balance Resistance; Mixing; 5.8GHzRadio frequency; Front-ends receiver

Abstract: This paper discussed the design of a 0.18 m CMOS process 5.8GHz RF front-end circuit, and the simulation and experiment were carried out. The main circuit design are low noise amplifier and mixer, the noise amplifier is overlay architecture, and using dual output mode single input / transformer coupling; The mixer is double balanced resistive architecture, and the FET are used as local oscillator input, so this kind of design has the advantages of no need of the level of the impedance matching and high performance. Experimental results show that: When the intermediate frequency is 2 GHz, the noise index is 2.7 dB, the conversion gain is 6.3 dB, and the input of the three order breaking point is 11 dBm. 1.2 V supply voltage under the consumption of energy is 4.3 mW, and the chip area is 1.1 x 0.66mm^2. The design of this chip can be widely used in the microwave electronic toll collection system.

1 Introduction

Dedicated Short Range Communications（DSRC）is a kind of the intelligent transportation system, particularly suitable for vehicle information exchange and security warning purposes. For examples, electronic toll collection, electronic map data download, or even the vehicle automatic detection of collision avoidance and security, which are increasingly used. But the current international has not yet developed a global common specifications for the DSRC. Therefore, every countries are developing their own standards, such as ARIB in Japan, CEN in Europe and ASTM in the United States, and the use of frequency division duplex operation in China, that is, the transmission and reception for different frequency bands, Taking the vehicle engine as an example, the launch frequency is 5780 MHz ~ 5800 MHz, the receiving frequency is 5820 ~5840 MHz MHz, the maximum transmission power is 10 dBm, the receiving sensitivity is at least 70 dBm [1]. The key components of the DSRC/ETC system includes the integration of RF / baseband chip, the communication plus / decryption chip and the IC card control chip, and the low noise amplifier RF front-end with reduced frequency mixer has undoubtedly directly determines the receiving sensitivity of the system. In DSRC/ETC applications and its specification generally, the power supply requirements are not particularly, but cost considerations is a major factor. In this paper, the 5.8 ETC GHz receiver uses two times the frequency drop / frequency rise, as shown in Figure 1, the first intermediate frequency receiver is 2 GHz, the second intermediate frequency is 40MHz, using this architecture makes the system have better receiver sensitivity, and significantly reduce the RF frequency synthesizer design complexity and frequency accuracy requirements and can make RF chip integration in CMOS process [2].

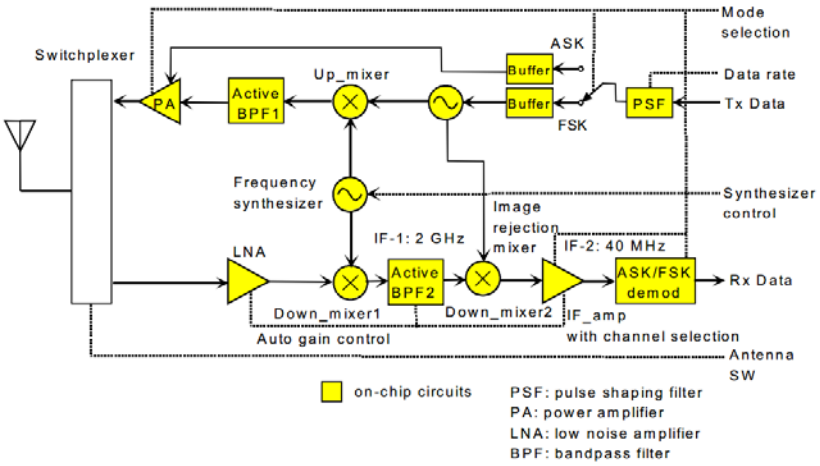


Fig. 1: The architecture of 5.8 GHz RF transceiver

2 Circuit design

2.1 Circuit design of low noise amplifier

Low noise amplifier is using overlay architecture, because the input / output has good isolation degree, the input matching can be devoted to the noise index and the gain, and the output impedance can be designed independently, and the low noise amplifier can be matched with the input of the next stage mixer, and the additional function of band-pass filter can be added. Design and selection is the common source level FET gate width, according to the empirical formula [3]

$$W = \frac{1}{3\omega L C_{ox} R_S} \qquad (1)$$

Where：L, C_{ox}—Respectively, the length of the FET gate and the unit capacity, RS for the power supply resistance, generally 50.

The input impedance of the L2 is adjusted by the source of the reduced inductance [4]

$$Z_{in} = g_m \frac{L_2}{C_{gs}} + j(\omega L_2 - \frac{1}{\omega C_{gs}}) \qquad (2)$$

Where： g_m, C_{gs}—Transduction and gate - source capacitance of FET, respectively.

The input resistance of the part of the use of L2 to 50, the imaginary part of the reactance component compensation (usually in series with the inductor), the minimum noise index will be higher than the original, the expression is[3]

$$F_{\min,l} = F_{\min} + \omega \frac{C_{gs}}{g_m}(2.4\frac{\gamma}{\alpha} - 2.3) \qquad (3)$$

Where：γ— the channel noise ratio constant, generally is about 2. α = g_m /gd0 ,for DS at zero bias voltage, the general α value is about 0.85. Will (3) the g_m / Cgs approximation for the ω_T, Then (3) can be simplified as:

$$F_{\min,l} = F_{\min} + 3.35\frac{\omega}{\omega_T} \qquad (4)$$

As long as the operating frequency is FET unit current gain bandwidth ω_T more than 10 times higher, increased noise index is not too much. The double balanced structure of the next stage mixer should be considered in the output end of the overlapped circuit. The signal must be converted to the differential type, direct voltage, single end differential and impedance conjugate matching between the two stages are directly applied to the chip transformer with a center tap. At the same time, the parallel capacitor C3 can be used in the primary coil to further make the tuning circuit, which can achieve the purpose of partial band pass filtering. At the base of the extreme, the load impedance is

$$Z_L = (\frac{1}{j\omega C_3}) \left\| [(r_p + j\omega L_p) + \frac{(\omega M)^2}{(r_s + j\omega L_s) + Z_{in,mixer}}] \right. \quad (5)$$

The Z_L can be adjusted to overlap type circuit of common gate pole conjugate output impedance and get the maximum signal transmission.

2.2 The mixer

Down mixer intended to use a similar Gilbert-cell architecture, as a double balance operation, but the design methods of mixing into resistive, in order to obtain the better index and IP3 noise characteristics[5].The bias mode is completed by the current source mode, and the local oscillation signal is injected at both ends of the base / source to facilitate the reduction of the power consumption of the base signal drive mode, at the same time, the power required to drive down the local oscillation[6]-[7]. The circuit architecture is shown in figure 2, M1~M4 for the mixer core, M5 and M6 for the active load, M1~M6 bias current source is provided by the M7/M8, C1 and C2 is DC blocking capacitors, the final output is removed from the base of the M1/M3 and M2/M4. Differential input local oscillator connected to the FET substrate and the source, the critical voltage Vt is changed as follows:

$$V_t = V_{t0} + \gamma[\sqrt{2\phi_F - v_{LO}(t)} - \sqrt{2\phi_F}] \quad (6)$$

If we designed the M1~M4 operating in the triode, the base source conductance

$$g_{DS} = k_n^{'} \frac{W}{L}[v_{GS} - V_t(v_{LO})] \quad (7)$$

When the gate DC bias is close to the critical voltage, the local oscillation signal drives the FET to form a time varying resistor with a variable frequency of f_{LO}. For the simple design, it is assumed that the conductance of the base - source can be changed between 0 and g_{ON}, and the base - source can be regarded as a time - varying resistor controlled by the gate electrode. Its current is

$$i_D(t) = g_{DS}(t) \cdot v_{GS}(t) = \frac{\pi}{4} g_{ON}[\cos\omega_{LO}t - \frac{1}{3}\cos 3\omega_{LO}t + \text{L}\ ] \cdot v_{GS}(t) \quad (8)$$

And RF signal is applied in the gate terminal, so the base current with mixing, double balanced architecture can eliminate some of the clutter, especially I stray waves can completely be eliminated, let triode between isolation effect is better. Must pay attention is that injected local oscillation signal substrate / source at both ends, the threshold voltage Vt, FET source terminal voltage is low, prompted v_{GS} values were greater. In other words, you cannot be a local oscillation signal much the operation between FET to two different conductance values. So the local oscillation signal power required of the whole system is reduced.

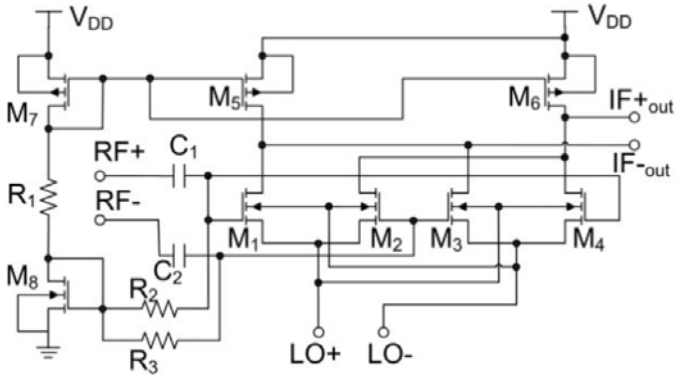


Fig. 2: Down mixer of 5.8 GHz

3 Simulation and measurement results analysis

3.1 Chip transformer

The chip transformer has an absolute influence on the performance of the whole circuit, so the design and simulation of the chip must be particularly careful, so that the coupling coefficient can be improved. Chip transformer using winding stacked method, a total of three laps, the number of

laps is1: 1, and the center tapped ground mode for single end turn differential signal[5]. Using Momentum Agilent for electromagnetic simulation, and get the differential S parameters such as the self-inductance, transformer chip quantity, quality factor, coupling coefficient and real circle number ratio. The simulation results of these parameters on the frequency scan are shown in Figure 3, self-inductance value at 5.8 GHz is about 1.1 nH and two coil Q value at 5.8 GHz are 6.9 and 2.7, coupling coefficient is 0.82, the number of turns ratio is1.02. As for the overall circuit simulation, the electromagnetic simulation of four S parameters of direct substitution and DC characteristics section is to and ideal for RF containment circle flow simulation.

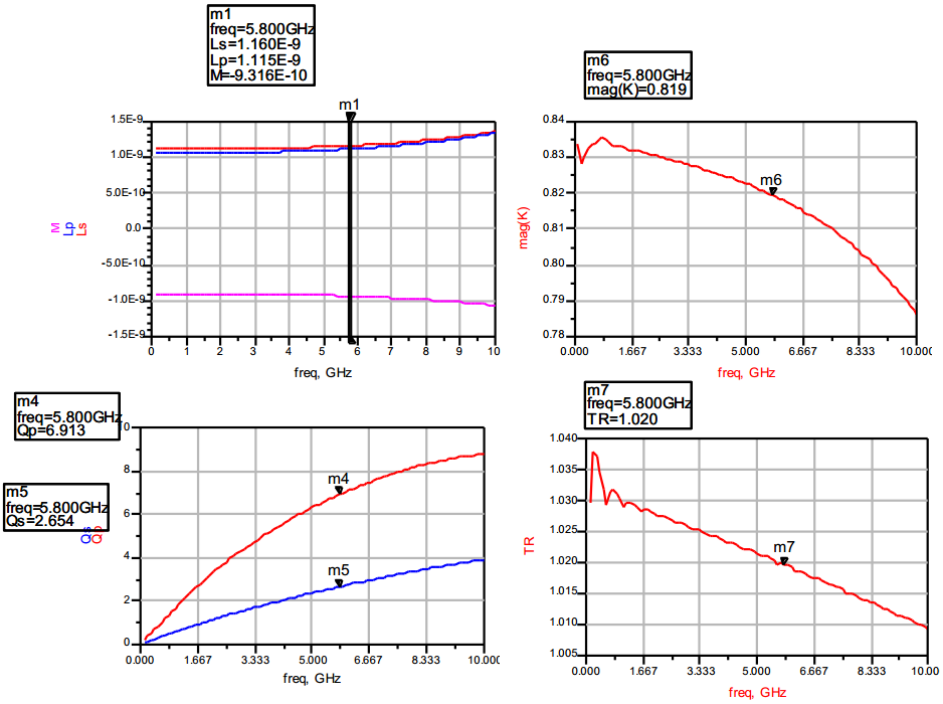


Fig. 3: Simulation results of the chip transformer

3.2 Overall circuit performance

In the whole electrical circuit of the parts, using of ADS Agilent and Momentum to complete the circuit simulation design, using CMOS TSMCRF 018 M model for Pre-layout simulation, and consider the overall chip to walk the line, adding Post-layout simulation, as well as the model of the RF test point effect. In small signal simulation, will observe the conversion gain, noise index, input reflection coefficient, in the large signal simulation, will observe the performance of the input of the three point of the broken point (IIP3). Simulation of the power supply voltage is set to 1.2 V, the local oscillation power is set to 5 dBm. The simulation results show that in RF signal for 5.8 GHz, the intermediate frequency signal of 2.0 GHz of the conversion gain is 6.3 dB and noise figure is about 2.7dB, input reflection within the frequency band of operation all less than 10 dB, the overall power consumption of the circuit is about 4.3mW. There is little difference between Pre-sim and Post-sim, the whole RF front end circuit should be able to meet the requirements of the microwave electronic charging system.

3.3 Chip routing and application testing

The chip of this RF front-end circuit is shown in Figure 4, the area is 1.1 x 0.66mm^2.The left end is the wafer RF input, the right end is the intermediate frequency output, above is the local oscillation differential input, below for DC power supply and the control signal ends. The chip using wafer probe measurements directly on the wafer, except the noise index, all the other parameters measurement architecture as shown in Figure 5, The probe RF input using the standard G-S -G configuration of 100 μ m distance, which is a P-G-P-P-G-P type. LO and IF side using the plug-in Balun to provide differential signals, Balun using Model Inverting 5100 Transformer Picosecond, operating frequency of 200 kHz to 23 GHz, in 2 GHz about 6 dB of the loss. RF and LO end use analog signal generator to provide measurement input signal, IF end use spectrum analyzer to observe the output spectrum. Noise figure measurement architecture as shown in Figure

6, the same as used in Agilent E4440A. Due to the use of external balun, so that the measurement to the noise index for material with output balun results to be measured, but can be corrected off input line of the transmission line loss. All circuit characteristics are measured at the high frequency technology center of the nano element Laboratory (NDL).

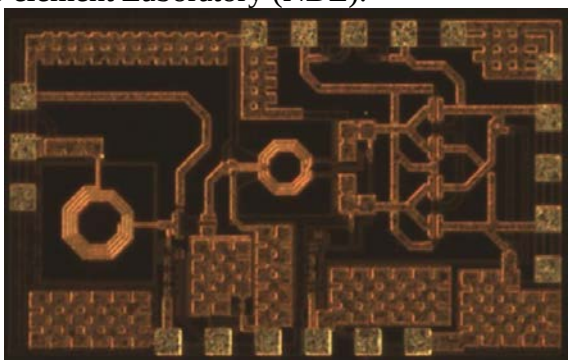


Fig. 4 Circuit chip of RF front end

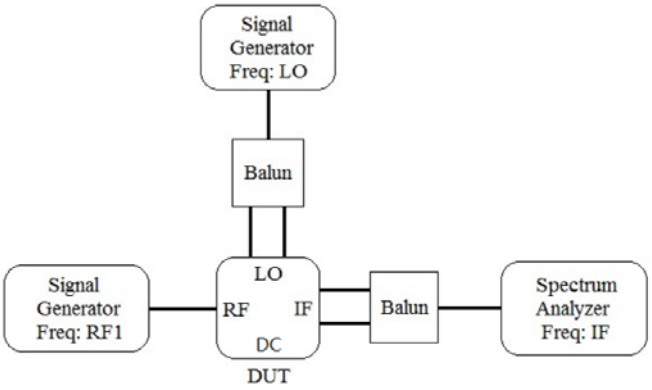


Fig. 5 General parameter measurement architecture of RF front end circuit

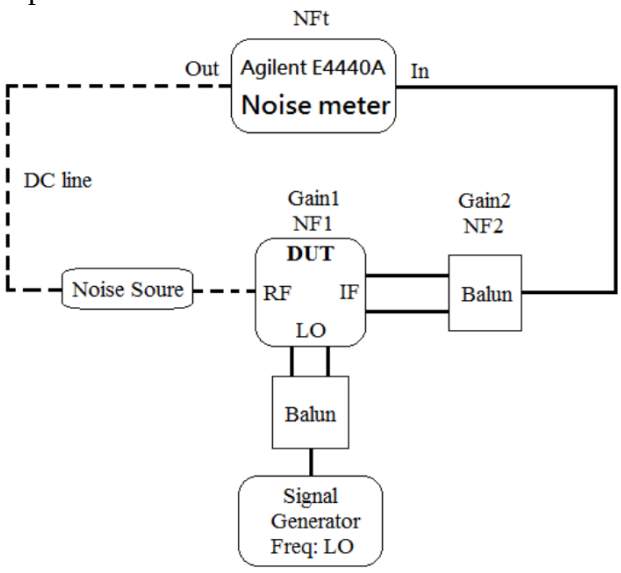
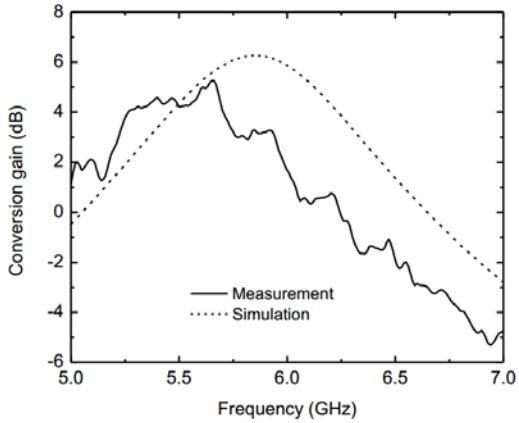


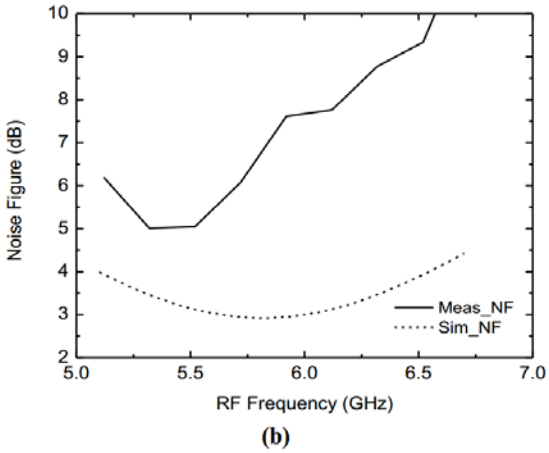
Fig. 6 Noise signal index measurement architecture of the radio frequency front end circuit

3.4 Comparison of simulation and measurement

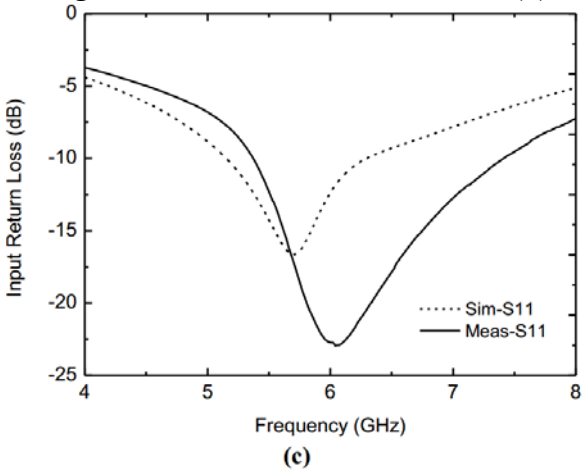
Figure 7 (a) is the RF frequency conversion gain of the scan map, at this time the frequency of RF scanning is 5 GHz to 7 GHz, The LO scanning frequency is 2.92 GHz to 4.93 GHz, and the fixed IF frequency is 2.07 GHz. Figure 7 (b) are the simulation and measurement results of noise index, At this time, the fixed LO frequency is 3.72GHz, the frequency of RF scanning is 5.12 GHz to 6.72 GHz, and the IF frequency is 1 GHz to 3 GHz. Figure 7 (c) are the simulation and measurement results for the input end reflection coefficient S11, Table 1 is the measurement and simulation comparison summary, if balun loss, the conversion gain little difference and noise index has a high phenomenon.



(a) Conversion gain



(b) Noise index



(c) The input reflection coefficient

Table 1 Simulation and measurement results of RF front end circuit

Parameter	Specification	Simulation	Measurement
Frequency (GHz)	5.8	5.8	5.8
Noise figure (dB)	< 4	2.8	6.1
Conversion gain (dB)	>5	6.3	3.9
S_{11} (dB)	<-10	-15	-20
DC power (mW)	<5	4.3	5
IIP3 (dBm)	>-15	-12	-12
Chip Size (mm^2)	<1.2x0.7	1.1×0.66	

4 Conclusions

This paper designed a 5.8GHz RF front-end receiver based on double balanced resistive mixer. The main circuit design are low noise amplifier and mixer, the noise amplifier is overlay architecture, and using dual output mode single input / transformer coupling; The mixer is double balanced resistive architecture, and the FET are used as local oscillator input, so this kind of design has the advantages of no need of the level of the impedance matching and high performance. The circuit design is also tested by simulation and experiment. Through the study we can get the following conclusions: When the intermediate frequency is 2 GHz, the noise index is 2.7 dB, the conversion gain is 6.3 dB, and the input of the three order breaking point is 11 dBm. 1.2 V supply voltage under the consumption of energy is 4.3 mW, and the chip area is 1.1 x 0.66mm^2. It can be widely used in the electronic toll collection, electronic map data download, and the vehicle automatic detection of collision avoidance and security.

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