Research on the High Speed Image Transfer based on the Zynq-7000

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Abstract. Transferring Image data and Video data will expend a lot of bandwidth.this article raise an AXI DMA high speed communication interface design based on Zynq-7000.Compared with traditional DSP+FPGA architecture,the new Zynq7000 has many superiority.such as low cost,low power,low develop difficulty,software and hardware re-custom.User can create a new IP as they want.this method decreases the number of digital IC and devices.This system use AXI DMA interface as a bridge communicating with DDR3 SDRAM and FPGA.On the basis of test,the speed of AXI DMA interface can reach 298MB/s.it can absolutely replace traditional Serial RapidIO and EMIF(External Memory Interface)in DSP+FPGA architecture.

Introduction

Nowadays,Embedded System has developed rapidly,There are a lot of demand cannot be meet with existing products.Existing products containing a single processor, a single ARM, or a simple FPGA program has been unable to meet the demand of user.Insight into the next generation of embedded processors, we will find that improve performance, reduce costs, reduce the power consumption, narrow shape, increase flexibility is its main demand.Although existing FPGA + DSP platform is the first choice for many signal processing, but the ARM and DSP processor and FPGA processor have different architecture, programming model , this creates both sides communication need complex interfaces and protocols to ensure that.

Commonly used DSP and FPGA processor communication interface are External memory interface and serial Rapid IO interface.Though the two interfaces on the communication speed can meet the needs of users, but the complicated communication protocol should be guarantee by both developers , this also caused the development cycle longer difficult.Therefore, Xilinx launched Zynq SoC platform with ARM + FPGA architecture.we call ARM parts Processing System (Processing System), hereinafter referred to as PS.We call FPGA parts Processing Logic (Processing Logic), hereinafter referred to as PL.

This paper discusses a new way of data transmission, which is PL uses the AXI DMA communication IP core for high-speed image data transmission, and save the data to DDR3 SDRAM.This way advantages of high speed data transmission has the following several aspects: 1, the transmission speed, it uses AXI DMA control Zynq7000 AXI HP bus for high-speed data transmission, the transmission speed can reach 300 MB/s.2, adopted the AXI communication protocol between the FPGA and ARM, FPGA side of AXI DMA IP core can be controlled by the ARM, is equivalent to the ARM of a peripheral, so only need one ARM developers can complete the high-speed communication.After test, based on the AXI Zynq7000 DMA interface communication system is stable and reliable and high efficiency, it will be the first choice for the next generation of high-speed Internet interface.

System Design

At present Zynq-7000 structure map custom Logic and software respectively to PL (Processing

Logic) and PS (Processing System), and constructs a SoC design platform which uses the ARM as the controller core and the FPGA IP as powerful peripherals.Communication between FPGA and ARM use AXI Internet interface, AXI interconnection agreement is based on AMBA derived a new generation for SoC IP Internet protocol specification.Between PS and PL there are two kinds of general interface, the first is the AXI_HP interface, this is a high-performance port for high-speed data transmission.The second is the AXI_GP interface, this is a general control port between PS and PL.AXI GP interface is divided into AXI GP0 and AXI GP1 two interfaces, altogether has 2GB address space, any IP core costumed in PL will assign to random address in the address space, thus the IP core is used as a peripheral can controlled by the program.Figure 1 shows the structure schematic diagram of the system,The system contains the links as follows.the AXI DMA slave port connected to the PS general main port 0 (M_AXI_GP0).PS uses the port to configure registers, which are used for data transfer and check status.

1) AXI DMA master port connect to the PS side high performance slave port 0 (S_AXI_HP0).AXI -DMA write data to the DDR memory .It is used for the purpose of DMA data transmission buffer.
2) In PL part structure,we can use increasing data generator pl_dma_0 IP core to generate data, then sent incremental data to the AXI DMA, here we can use AXI DMA as a controlled water pipe, a steady stream of incremental data generator sends the data to AXI DMA, AXI DMA controls a certain amount of (0x800000MB is largest) data that is sent to DDR3 SDRAM.So this operation finish a PL write data to DDR3 SDRAM operation.
3) In order to guarantee communication perfectly, we can add GPIO IP core on the PL part, it is used to make handshake signals between AXI-DMA and pl_dma_0.PS can control both the AXI DMA and GPIO both IP core, the system assigned to the two IP core address randomly.
4) After finished the amount of data AXI-DMA specified or data transmission error in the process of the transmission , it will trigger the AXI DMA interrupt,The interrupt will inform cortexA9 core0 in PS part,and then it will reach interrupt handling.The system block diagram as shown as follows.

Note:

the diagram is corresponding IP core and PS with the main connection diagram, in order to make it easy for readers to read, it does not connect the lines to the clock and reset.the axi -mem-intercon and processing system7-0-axi-periph are derived for systems interconnection, the axi_mem_intercon and processing_system7_0_axi_periph are derived for systems interconnection, the former is used as M_AXI_S2MM master interface and the S_AXI_HP0 is used as the slave interface of data between the bridge of the Internet.The latter is used as the master interface and S_AXI M_AXI_GP, S_AXI_Lite and S00_AXI control interconnection bridge, were used to configure GPIO, AXI DMA, pl_dma_0 work mode and working condition.

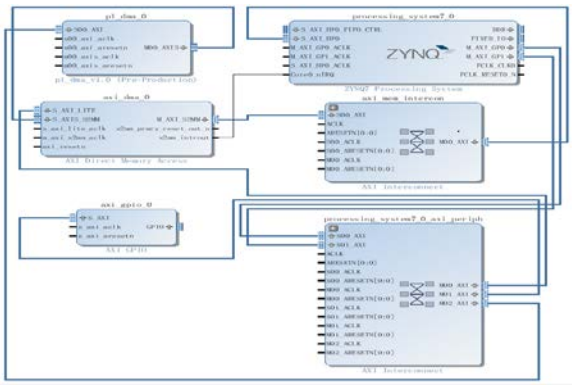

Figure 1. Overall system structure

Interface Design

AXI DMA Interface configuration. Xilinx SoC platform for the development of software has

been updated to latest Vivado,at present the latest version of the Vivado is 2015-2.For using Vivado, this article is no need to do extra explain, readers can go online to find.Open the Vivado interface, add the DMA IP core in the IP Integrator , after the completion of adding as shown in figure2.

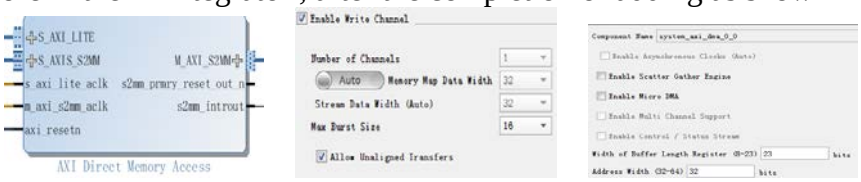

Figure2. AXI DMA Configuration

Double-click the IP module, you will see as shown in figure 2-2 and the configuration of the interface shown in figure2.Simple transmission mode is used in this article, thus do not need to choose Enable Scatter Gather Engine mode.Max Burst Size is Burst transmission interval Size , it specifies the maximum burst transmission cycle.Here,we can reserve default parameter settings.The option of the Width of Buffer Length Register, choose the biggest 23, ensure that the AXI DMA can send 0x800000 amount of data.The rest operation can according to the default settings.AXI DMA IP core is quite to FPGA IP core which developers have write out successfully, some configurable parameters ports and several configuration data ports have been reserved, and then users can configure IP modules working parameters, to meet the needs of users.

GPIO Interface configuration. Also,Users can add the AXI GPIO IP core in the IP Integrator,When completed,it is as shown in Figure3.AXI GPIO configuration is relatively simple.Because we only use one bit GPIO,so we write 1 to the GPIO Width blank.then we choose All Output to make the one bit GPIO to a output direction.

Figure3. AXI GPIO Configuration

PS Processor Configuration. Also,it can add the AXI Zynq7000 PS IP core in the IP Integrator,When completed,it is as shown in Figure4.

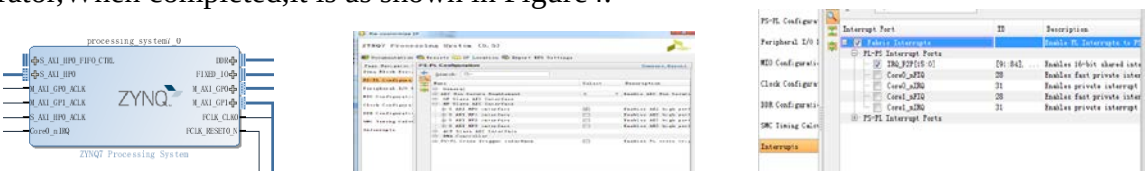

Figure4. AXI Zynq 7000 PS Configuration

At First, in PS - PL Configure options choose the HP Slave AXI Interface option, then we choose S_AXI_HP0 AXI Interface to used data path between the DMA and DDR3 SDRAM.Then,in the Interrupts options we check Fabric Interrupts and choose cor0_nIRQ interrupt, this is core0 31 interrupt in PS part,it is directly received the AXI S2MM_introut the pins of the DMA, used for receiving the interrupt.

According to the above interface design, we can summarize as follows: Xilinx create many IP cores for users to call, this operation convert software interface into the work of all hardware modular work,Users can in directly call IP core and then connect them in Vivado platform,and then write the upper application in the SDK software.This choice simplify the development cycle.

Software Design

Xilinx Vivado platform provides a series patterns to convert the development environment from hardware to software SDK support scheme.After completing the hardware platform which introduced in article above,you can export the bit stream file, and then launch the software development platform SDK.Software development platform SDK is based on the Eclipse architecture development environment.the development is easy to use.After exported the bit stream,we can establish new project called PS_PL_AXIDMA in the SDK, and import the consistent

hardware platform of BSP support package.As shown in the figure below:

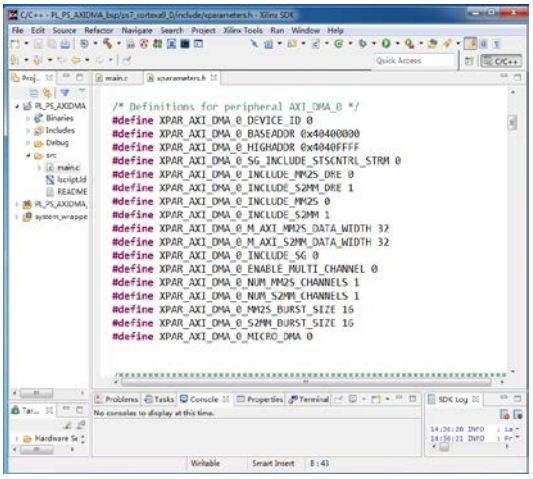

Figure5. Software SDK development environment

Among them, the only associated hardware platform and software platform is inside the BSP packet named as xparameters.h.this header file records the various IP and ID number and the base address of built-in peripherals PS,it is the principle of PS part operate PL part and its own IO peripheral.As picture above, a new platform for the AXI DMA assigned a unique ID number and the base address, according to the hardware platform configuration parameters and automatic generation a macro definition file here.The main function is used to operate the IP core.

Software Process

First of all, the ARM application need to initiate IP core of AXI DMA, this operation need to configure the AXI DMA interrupt and read the AXI ID number of the DMA and macro definition parameters to initialize the AXI DMA.And then software will initialize AXI GPIO,and it will be configured as output direction,used for handshake signals between PS and PL.when Initialization is completed,the PS part inform the PL pl_dma_0 part through GPIO sends a from high to low pulse to inform pl_dma_0 IP core for incremental data.Then data from pl_dma_0 flows through AXI DMA to DDR3 SDRAM.After a specified number of data through the AXI DMA, it triggers the DMA interrupt, notify the PS side that data volume has reached the DDR3 SDRAM.Then such a reciprocating tested data transmission.The software block diagram is shown in figure6.

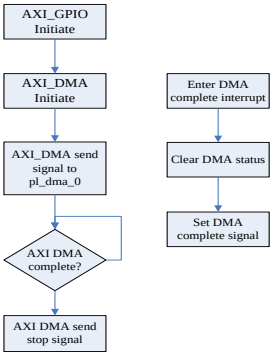

Figure6. Program flow picture

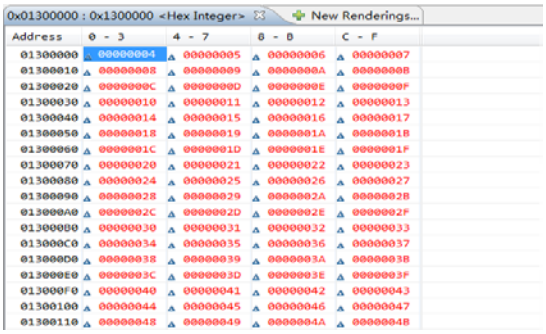

Figure7. Test result

System test.

When AXI DMA completed interrupt approached,We can see the data in the DDR3 address just like Figure7.After many tests, and modify the test data, get the following table:

Table1:Test Result

Test Data quantity	Test Result	DMA transfer speed
64KB	Increment OK	285MB/s
1MB	Increment OK	279MB/s
4MB	Increment OK	269MB/s

Conclusion

Through the above tests, we can get the following conclusions: based on the basis of AXI Zynq7000 DMA high-speed communication system is the first choice for the next generation communication system.It can replace the traditional DSP and FPGA structure to build communication system.No matter from the function or performance, AXI DMA can replace serial RapidIO and the external memory bus (EMIF).And in the Zynq7000 ARM + FPGA architecture can reduce the board, save the development cycle, save resources.It will become the future SoC that electronic engineers looking forward to.In addition, the characteristic that the hardware and software can customize will be an unique feature in Xilinx Zynq SoC.users do not need to buy a wide range of digital IC laid on their PCB, this process can completely by the FPGA developers themselves to the development of special digital IC or call Xilinx IP core is given.Then users can connect all kinds of IP core with PS,The communication systems will be laid.The rest of the work can be handed off to the ARM technical personnel development.

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