Analysis and Design of Charge Pump Configurations Based on Voltage Doubler for RFID

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Abstract.

Charge pump is the configuration which can provide a voltage gain to program nonvolatile memory in radio frequency identification (RFID). In this paper, A complete theory of charge pump is presented, which shows that the influence of body effect on power dissipation and power efficiency is more and more obvious. To solve this problem, a voltage doubler applying new body biasing is proposed, which has been implemented under 0.18μm CMOS process. The 10-stages proposed charge pump with pumping capacitor of 1pF at the clock of 2MHz can show a maximum power efficiency of 84%, in addition, it also can boost the voltage 1.8V input to 18.6V under 2μA output current successfully.

I. Introduction

RFID (radio frequency identification) technology as the key technology of the internet of things draw people's attention in recent years. Non-volatile memory is an indispensable component in RFID. The voltage provided in the RFID tag is low (<1.8V), but to write and erase the Non-volatile memory (NVM)requires high voltage (>10V)[1]. therefore, a efficient charge pump is necessary to boost the voltage of power supply to the required high voltage.

Charge pump is a capacitor based circuit in NVM, which provide a voltage gain. Basically, the Dickson charge pump[2] is the most traditional charge pump, because of the voltage threshold loss in every stage, it affects the efficiency of charge pump seriously. To solve this problem, some new configurations are putted forward. The gate-crossing voltage doubler is one of them. The voltage doubler is a kind of charge pump that based on cross-coupled NMOS transistors and pumping capacitor which is introduced in [3]. However, the efficiency is still limited due to the bulk effect. The bulk effect always affect badly the performance of the voltage doubler, this paper present voltage doubler with a new type of body biasing, it not only can provide reverse bias of the junctions, but also can eliminate the bulk effect. The simulation results show that the proposed charge pump can successfully boost the voltage 1.8V input to 18.6V under 2μA output current, it is sufficient to drive the load to required voltage.

II. Overview charge pump circuit

Charge pump which also known as switch capacitor voltage converter is a DC-DC conventer that pumping charge with capacitance. The Dickson charge pump is widely used in NVM for many

years, In this section, We will introduce the theory of charge pump and give an overview of voltage pump.

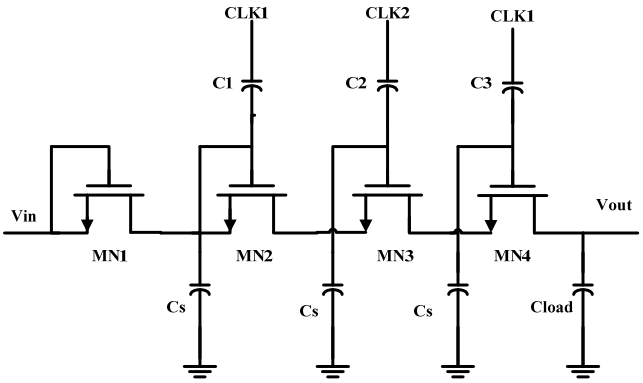

Fig.1 The Dickson Charge Pump

The Dickson charge pump is composed of diode-connected NMOSFET which shows in Fig.1. In one clock period, the difference of voltage between node N and node N+1 relation as follows:

$$\Delta V = V_{N+1} - V_N = V'_{\emptyset} - V_{TH} \tag{1}$$

$V'_{\emptyset}$ is the admeasure between coupling capacitance and autoeciousness capacitance.

$$V'_{\emptyset} = \left(\frac{C}{C+C_S}\right) V_{\emptyset} \tag{2}$$

Considered the status in practice, a part of current will be removed by load, accordingly arise the reduction of output voltage, the output current at clock frequency f as follows:

$$I_{OUT} = f(C + C_S)V_L \tag{3}$$

Considered the load current, the output voltage can show as that:

$$V_{out} = V_{DD} + N\left[\left(\frac{C}{C+C_S}\right) V_{\emptyset} - V_{TH} - \frac{I_{OUT}}{f(C+C_S)}\right] - V_{TH} \tag{4}$$

We can transform the V_{out} as follows：

$$V_{out} = V_o - I_{OUT}R_S \tag{5}$$

$$V_o = V_{DD} + N\left[\left(\frac{C}{C+C_S}\right) V_{\emptyset} - V_{TH}\right] - V_{TH} \tag{6}$$

$$R_S = \frac{N}{f(C+C_S)} \tag{7}$$

V_o is the open circuit output voltage, R_S is the output resistance. We can simplify the circuit of charge pump like Fig.2：

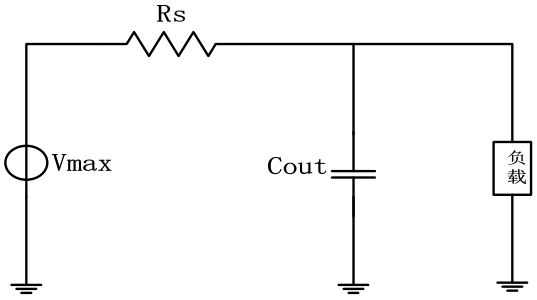

Fig.2 charge pump simplify figure

As the increase of stage, the voltage of the source increases constantly, but the voltage of the body is always grounding, so substrate bias voltage V_{SB} will gradually increase. The voltage threshold V_{TH} value loss will influence the voltage conversion efficiency and the power conversion efficiency seriously. If we use PMOS as the switch diode, it can take the appropriate body offset to reduce bulk effect, however PMOS as the switch diode needs more width. Thus it can be seen we should solve the voltage threshold value loss and bulk effect, therefore can acquire high voltage conversion efficiency and the power conversion efficiency.

III. The proposed voltage doubler

The voltage doubler is a kind of charge pump that based on cross-coupled NMOS transistors and pumping capacitor which is introduced in [4], we can see the cross-coupled NMOS transistors are driven by output of 2 phases clock to obtain pumped voltage , a dual series load switches composed with PMOS transistors as a single output connected together as the output of the cell shows in Fig3, it is aimed at avoiding the large drop of the threshold voltage.

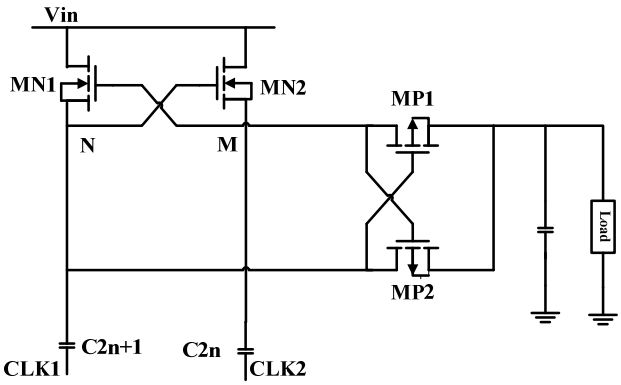

Fig.3 The Voltage Doubler

We can see the potential of the initial node N and M is 0, when CLK1 change from 0 to V_{DD}, the potential of the node N change to V_{DD} because of the C_{2n+1} capacitive coupling, MN_2 turns on , V_{DD} charging for C_{2n} through MN_2, the node M charge to $V_{DD} - V_{TH}$.

when CLK2 change from 0 to V_{DD}, the potential of node M change to $2V_{DD} - V_{TH}$ because of the C_{2n} capacitive coupling, MN_1 turns on , V_{DD} charging for C_{2n+1} through MN_1, the node N charge to V_{DD}.

when CLK change from 0 to V_{DD}, the potential of node N change to $2V_{DD}$, MP_2 as the switche turns on, so the potential of node N can transmit to V_{OUT}. It can be seen form the above process, node N and node M alternate output $2V_{DD}$, the Gate cross-coupled circuit composed PMOS switches chooses the higher voltage of node N and node M output V_{OUT}. We eliminate threshold voltage value loss through elevating the gate voltage.

The voltage doubler use cross-coupled NMOS transistors, it can have higher carrier speed, a dual series load switches composed with PMOS transistors as a single output connected together to the each output of the cell, as the increase of the stage, the voltage of the NMOS source rise rapidly, bulk effect seriously affect the pumping efficiency[5]. The most impotent problem is to ensure the reverse bias of junction because of using PMOS as switch. Since it is difficult to gather six different voltage which can meet the demand of each MOSFET source terminal. In order to solve this problem, we proposed the charge pump like Fig4 shows.

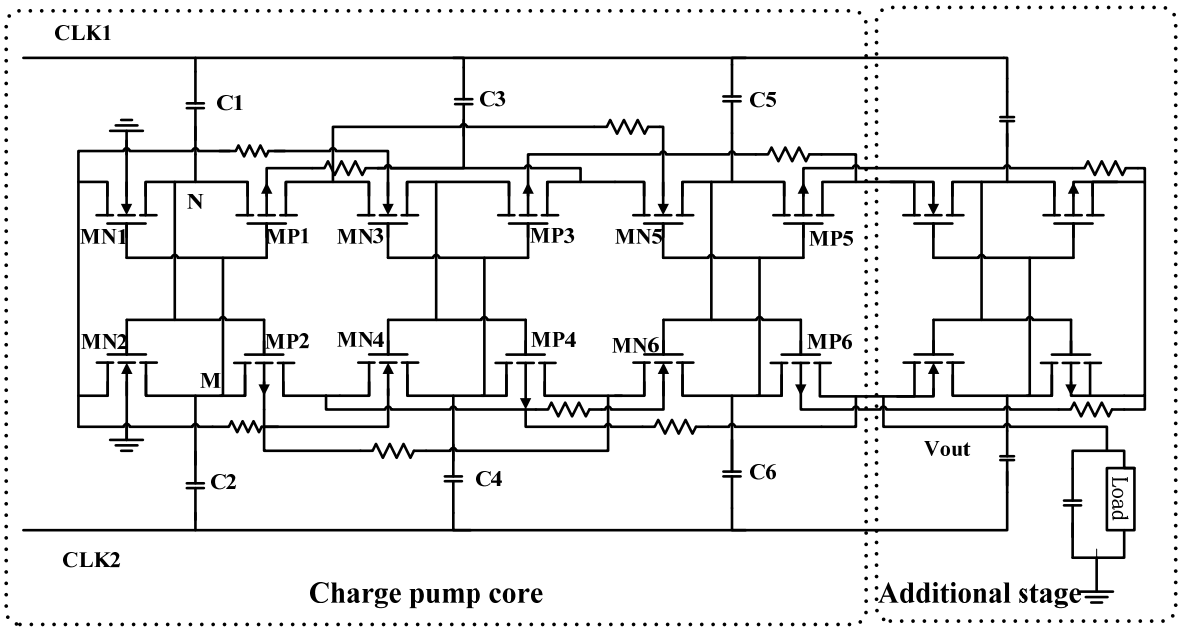

Fig4. Proposed 3-stage charge pump circuit with new body biasing

To eliminate the effect of the vertical bipolars, we connect the substrate of each PMOS to the next stage output voltage, in the same way, we connect we the substrate of NMOS to the previous stage input voltage. We use the resistor between the connection, it can reduce the leakage current, so that the power efficiency will also be optimized. Because there is no previous stage before the NMOS in first stage, the bodies of the NMOS are connected to ground. Since PMOS in the last stage we added an additional stage to provide the bulk voltage. In this way, it can avoid body effect, and make sure the PN junction reverse to prevent the leakage flow.

In the proposed charge pump, all the body of MOSFETs are connected to the terminal of charge pump itself in addition to an additional charge pump stage. This stage is made up of two small capacitance and four MOSFETs only to provide the body bias of the last stage with less than 1.5%.

Comparing to the conventional charge pump, the proposed charge pump circuit eliminate the threshold voltage loss, reduce body effect and make sure the PN junction reverse to prevent the leakage flow. It is particular worthy nothing that improve the power efficiency and reduce the power consumption.

IV. Experiment Results

The simulations of the proposed charge pump (10-stage as example) with new body biasing were all performed under 0.18μm CMOS process. Generally the voltage of CLK1 and CLK2 is the same with the power supply voltage (VDD). The frequency of the pumping clock is 2MHz. all the charge pump capacitance are 1pF, and the load capacitance is also 1pF.

The simulations output voltage of the proposed charge pump and the voltage doubler, the 4 phase clock charge pump under 1.8V input with the current increasing is shown in Fig5, it can be seen, the proposed charge pump can boost the voltage more efficiently as output current increases, the proposed charge pump achieved the higher gain compared with the other circuit.

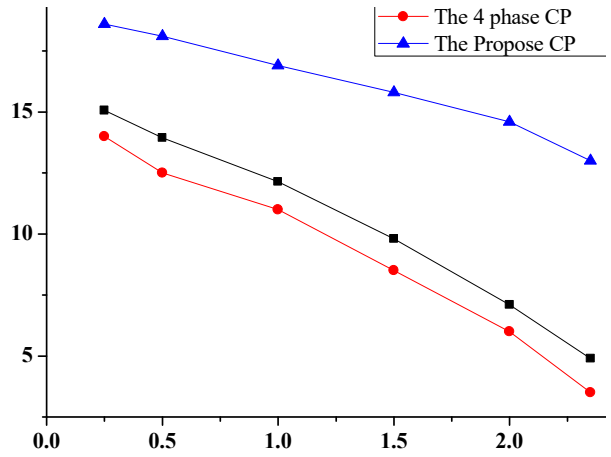

Fig5. Output voltage versus load current

Fig6 indicate the power conversion efficiency (PCE) of the 10-stage charge pump with various load current, as it shows, the PCE of the proposed charge pump is more efficient than the other circuit at the same load current. the maximum power efficiency is 84% with the load current of 0.5μA in this paper.

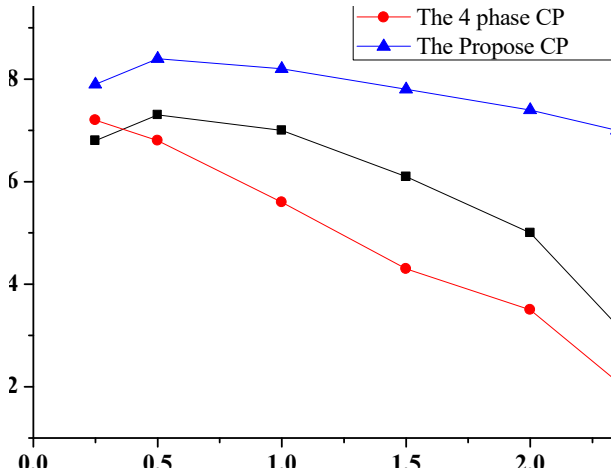

Fig6. Power efficiency versus load current

Fig7 shows the layout of the proposed circuit under 0.18μm CMOS process, the subsequent simulation as Fig8 have indicated that the presented circuit can provide the stable output voltage efficiently.

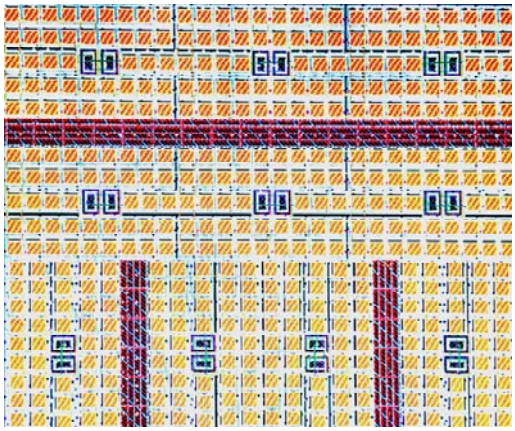

Fig7. Layout of the proposed circuit

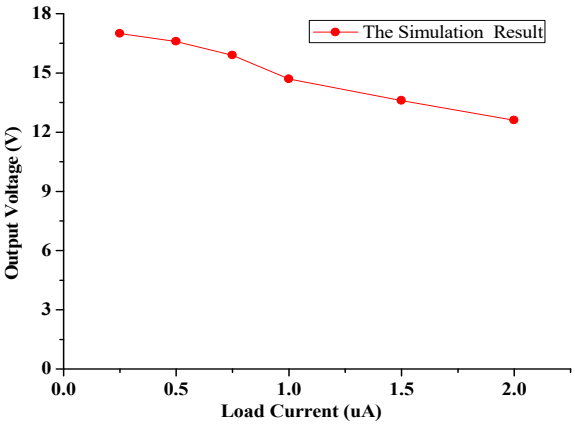

Fig8. Output voltage of simulation

V. Summary

A voltage doubler applying new body biasing with high power efficiency is proposed. The body biasing of the MOSFET is virtually eliminated and the configuration greatly reduce the leakage current. The charge pump is implemented in CMOS standard process, which shows high voltage conversion efficiency, power efficiency especially under large load current. Accordingly, the proposed circuit is suitable for RFID tag.

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