Adaptive Time Delay Compensation Realization for Remote Ship Main Engine Rotation Measurement

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Abstract. An adaptive time delay compensation algorithm has been developed based on thorough analysis of the integrated information transmission platform and the composition and characteristics of the time delay in V.35 channel, during which forward and reverse V.35 transmission channel has been developed properly. Combining AVR-microcontroller unit with Protothreads mutiple-thread technologies, automatic measurement and adaptive compensation of the transmission channel transmission delay is realized. The scheme does not need to change the time code terminal and just uses V.35 channel of integrated information transmission platform to transmit high precision time information, which can effectively reduce the demodulation error caused by signal distortion. Moreover, it also can simplify the wirting of the system and enhances the deployment flexibility of time code terminal.

Introduction

Ship main engine rotation speed mesurement is very important and there are already many different kinds of measurement method and instrument for engine rotation speed measuring or cylinder pressure measuring. In those methods opto-elemetronic method is used to measure the rotation speed, which is non-contact speed measuring method [1, 2]. Photoelectric speed sensor does not connect with the object to be measured and has no additional load, so photoelectric speed sensor with less measurement error and higher precision and the measurement capability is good. However, the precision is easily affected by timing. There are many methods compensating time delay [3-5]. A delay-dependent system is required to minimize transmission delay and error compensation [6]. Based on the adaptive time delay compensation circuit technologies [7-10], we firstly demstrated ship main engine rotation speed measuring setup and data acquisition terminal structure. Then data acquisition terminal input signal conditioning circuit, data acquisition terminal display interface circuit and data acquisition terminal internet interface circuit designation are designed in detail.

Hardware Design

According to the major functions of data acquisition terminal, there were four sensor interfaces, network interface, two display interfaces and a power supply module external interface. Considering the reliability and stability of system design, MCU embedded system design was adopted in the data collection terminal which was proved to be mature and reliable. The data acquisition terminal block diagram was shown in Fig. 1.
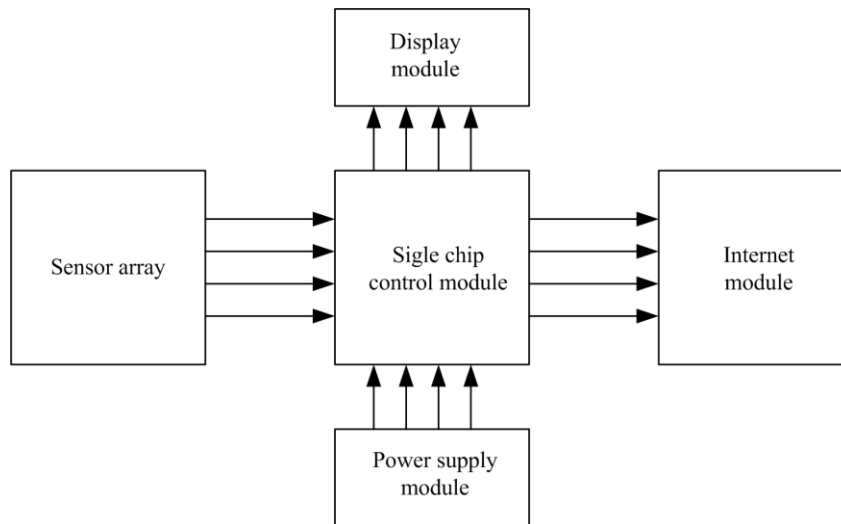
Figure 1. Data acquisition terminal block diagram

Data Acquisition Terminal Input Signal Conditioning Circuit Designation. Input signal conditioning circuit mainly acomplish the isolation between MCU and the input pulse, which also realizes the level conversion work. Input signal conditioning circuit diagram is shown in Fig. 2. Due to the active circuit design by using a speed sensor, the sensor output signal with open-collector (OC) interface design, a load resistance is required between the sensor signal and power supply to get output signal. The signal amplitude is 12 V close to the supply voltage. Moreover, both the computer's input and output interfaces are TTL level, but they can not be directly connected.
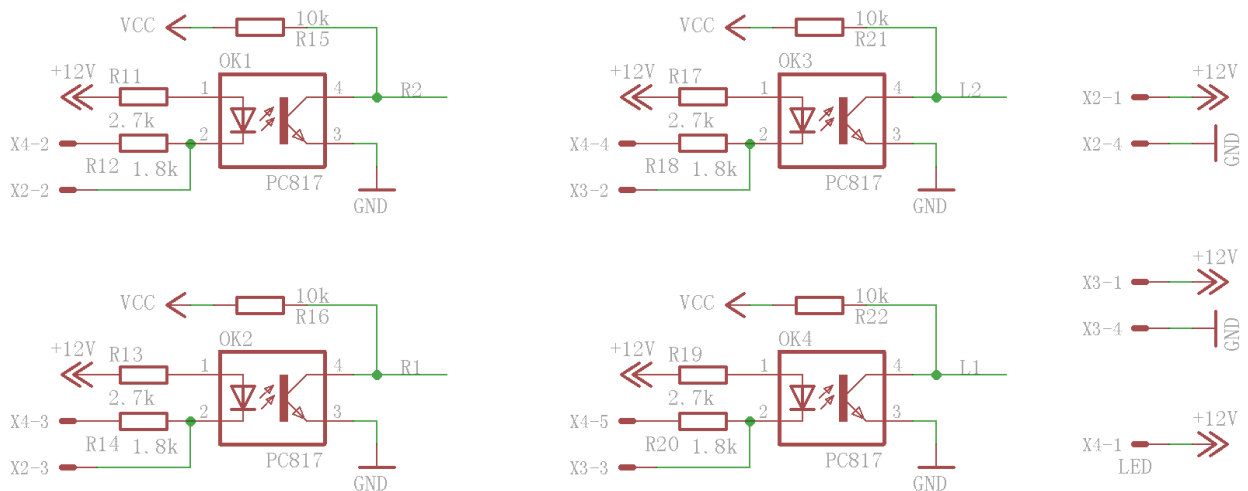

Figure 2. Schematic of data acquisition terminal input signal conditioning circuit

Data Acquisition Terminal Display Interface Circuit Designation. The display interface circuit mainly completes the level conversion work of the single chip microcomputer serial port output signal. Display interface circuit diagram is shown in Fig. 3. Because the serial port is the RS-232 interface, the microcontroller input and output interface can not be connected for the TTL level. So the level conversion circuit required to match each other. Considering the power supply voltage, operating current, anti-interference and circuit complexity, a product of company MAXIM named MAX3232 is selected as the interface conversion chip, which is a low-power duplex transceiver supporting 3.3 V power supply.
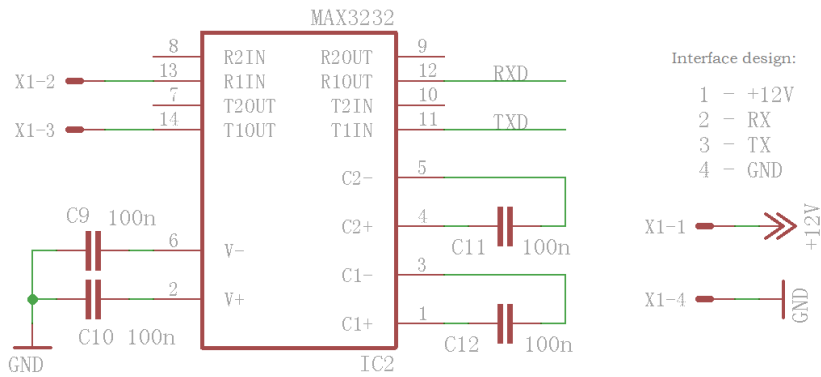
Figure 3. Data acquisition terminal display interface circuit

Data Acquisition Terminal Internet Interface Circuit Designation. Network interface is mainly used for remote command and data transmission, which has the advantage of speed fast, wiring simple, distance far compared to the traditional serial interface, but there are also weaknesses such as complex circuit and overhead network protocol. Easy circuit design and system stability should be considered in the selection of the network interface scheme. So network interface chip ENC28J60 which is a product of MicroChip is selected. Chip ENC28J60 adopts SPI interface with a microcontroller connecting, which is simple and fast. ENC28J60 has perfect functions of Ethernet, built-in 8K dual port RAM buffer to achieve the PHY layer and MAC media access control function, which conforms to the IEEE 802.3 standard. Both the independent clock circuit and peripheral circuit are simple, supporting 10 m duplex and simplex communication. The network interface circuit diagram is shown in Fig. 4.
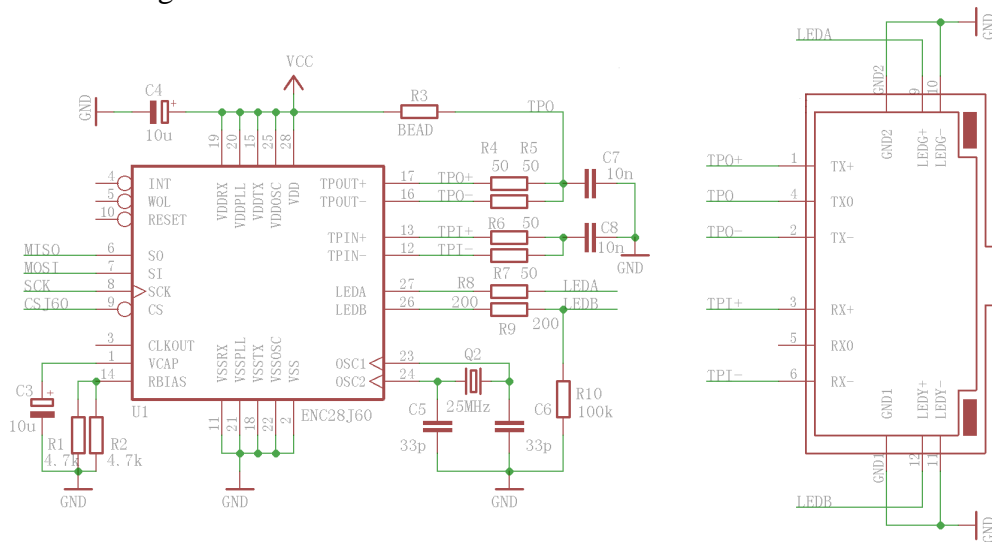

Figure 4. Data acquisition terminal internet interface circuit

Experimental Results

Schematic diagram of both forward and reverse channel delay testing and delay error compensation systems are shown in Fig. 5 (a) and (b).

Factors that affect the accuracy of the time delay compensation mainly include channel transmission delay jitter, MCU interrupt delay, instruction execution time, counter cycle count, transmission channel sampling error and bidirectional transmission asymmetry channel delay. The channel transmission delay jitter is far less than the transmission delay, which is generally tens to hundreds nano second not more than 1 us. MCU interrupt delay and the instruction execution time is a fixed value, which can be amended in SCM procedures with clock counter 1MHz. The cycle is one

microsecond, which is the same as maximum error of transmission channel sampling. In V.35 channel with 2048 kbit/s it is about 0.5 us. Because of SDH positive and reverse transmission channels in different time slots, it leads to the bidirectional delay being not exactly the same. By optimizing configuration methods, the asymmetry of less SDH bidirectional transmission channel delay can be reduced. Considering all of the above factors, the total error of time delay compensation is not more than 10 us. Experimental results of the transmission delay and error compensation are shown in Table 1.
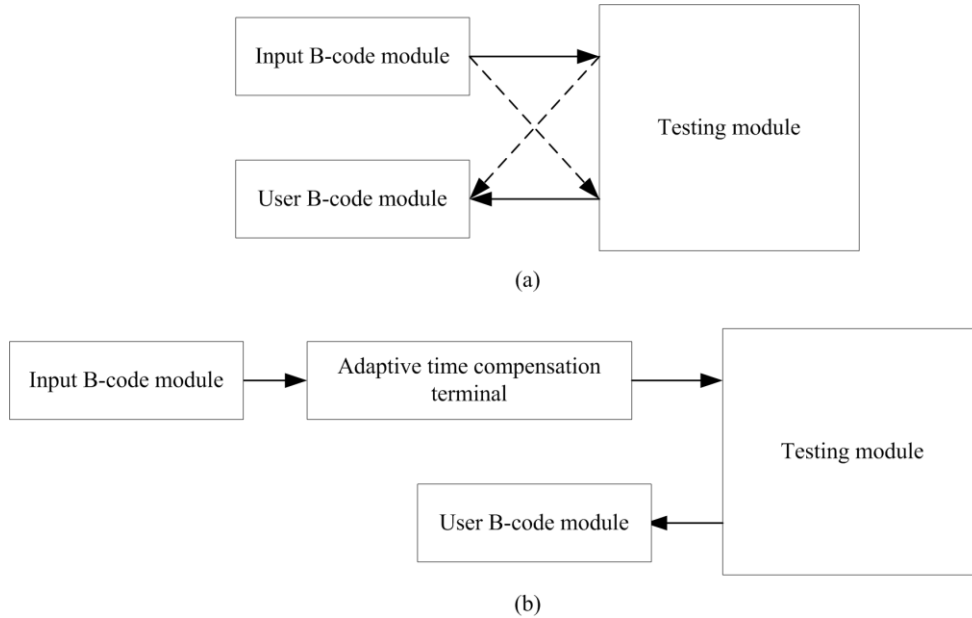

(a)

(b)

Figure 5. Schematic diagram of both forward and reverse channel delay testing and delay error compensation systems

Table 1 Experimental results of the transmission delay and error compensation

Testing item	Unit [us]
Forward channel delay	672
Reverse channel delay	670
Delay error compensation	<4
Delay jittering	<2

Conclusions

Based on the study of integrated information transmission platform, transmission delay composition and characteristics are analyzed in detai.High precision time information transmission scheme is proposed based on comprehensive information transmission platform of V.35 transmission channel. Through optimizing the allocation method of the transmission channel, optimal bidirectional symmetric V.35 configuration is obtained. Through analysis and research of B-code signal characteristics, the B code signal adaptive time delay compensation algorithm is put forward and proves to be suitable. Taking B code second signal as reference, adaptive time delay compensation algorithm is proposed, which is the basis for the adaptive time delay compensation. Based on AVR MCU and protothreads multithreading technology, transmission delay of the integrated information transmission platform automatic measurement, including B code decoding and encoding are realized.

The integrated information transmission platform V.35 transmission channel with high precision time information transmission is accomplished finally.

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