

Design and Implementation of Broad-Band Jamming Signal Source for GPS

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Abstract: The interference and anti-interference problem of GPS have great significance. This paper proposes a design of broad-band jamming signal source which is based on mixing LO and IF. LO signal is generated from signal generator ADF4351. IF signal is generated from amplifying and filtering the base noise. And the jamming source has simple structure and good performance.

The introduction

GPS satellite navigation system has been widely used in military and civil fields. According to the operational requirements, it is necessary to destroy the enemy's communications and navigation of GPS. So the research of GPS signal interference is more and more important[1][2]. This paper proposes a design of broad-band jamming signal source, which is based on signal generator ADF4351 and base noise. What's more, the jamming sources itself has simple structure and ease to implement and debug.

The overall structure of signal source

The output RF jamming signal is generated from mixing LO signal and IF noise signal. IF signal is generated from amplifying and filtering the base noise. The LO signal is generated from signal generator ADF4351. The data of ADF4351's registers is written and updated regularly by ARM. Because the frequency of LO can be changed by ADF4351, the central frequency of RF jamming signal can be controlled by program. The structure of jamming signal source is shown in Fig.1:

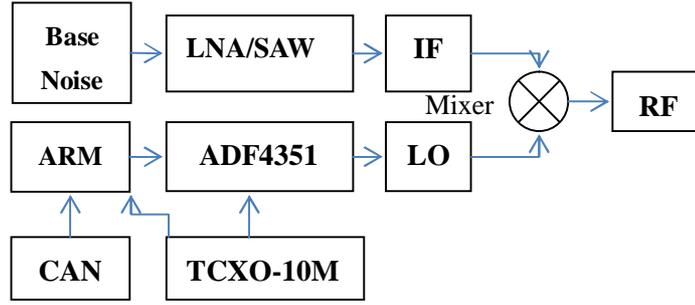


Fig.1. The structure of jamming source

The configuration of ADF4351

Introduction to ADF4351

The ADF4351 allows implementation of fractional-N or integer-N phase-locked loop (PLL) frequency synthesizers when used with an external loop filter and external reference frequency[4].

The ADF4351 has an integrated voltage controlled oscillator (VCO) with a fundamental output frequency ranging from 2200 MHz to 4400MHz. In addition, divide-by-1/-2/-4/-8/-16/-32/-64 circuits allow the user to generate RF output frequencies as low as 35MHz. Control of all on-chip registers is through a simple 3-wire interface[5]. The device operates with a power supply ranging from 3.0 V to 3.6 V and can be powered down when not in use.

Parameter design

The frequency and power of ADF4351 output Signal is determined by the parameters of registers [6][7]. According to the signal generator signal output formula programming as Eq. 1 and Eq. 2:

$$RF_{out} = \left[INT + \left(\frac{FRAC}{MOD} \right) \right] \times \left(\frac{f_{PFD}}{RFDIV} \right) \quad (1)$$

Where:

RF_{out} is the RF frequency output.

INT is the integer division factor.

$FRAC$ is the numerator of the fractional division (0 to $MOD - 1$).

MOD is the preset fractional modulus (2 to 4095).

$RFDIV$ is the output divider that divides down the VCO frequency.

$$f_{PFD} = REF_{in} \times \left[\frac{(1+D)}{R \times (1+T)} \right] \quad (2)$$

Where:

REF_{in} is the reference frequency input.

D is double bit (0 or 1).

R is reference division factor (1 to 1023).

T is the reference divide-by-2 bit (0 or 1).

According to the design requirements of the jamming source, external reference clock signal is 10MHz. And the center frequency of output RF signal is 1575.42MHz. The bandwidth is 4MHz. In order to generate the broad-band jamming signal, the frequency of LO signal is set to 1975MHz, the power of LO signal is set to 0dBm. Based on the demand, it is necessary to confirm the data of

registers.

Taking 1975MHz as an example to determine the design parameters: $RF_{out} = 1975\text{MHz}$; $REF_{in} = 10\text{MHz}$; $MOD = 25$; $D = 0$; $T = 0$; $R = 1$; $f_{PFD} = 10\text{MHz}$; $INT = 395$; $FRAC = 0$.

Where: $LO = RF_{out}$.

The data of registers are determined as shown:

R0 (00 C5 80 00)
R1 (08 00 01 91)
R2 (14 00 4E 42)
R3 (00 00 04 B3)
R4 (00 95 00 3C)
R5 (00 58 00 05)

The design of loop filter and its simulation

The design of loop filter is a key part of PLL design. In order to get a stable VCO control voltage, the loop filter should be used to filter the high frequency interference in the linear voltage[8].

In this paper, a passive two order low-pass loop filter is used. And the loop bandwidth is 20 kHz. The phase margin is 45 degrees. The value of capacitance and resistance can be determined by simulation software ADI-simPLL4.1 by ADI's company. The result is just as shown in Fig.2:

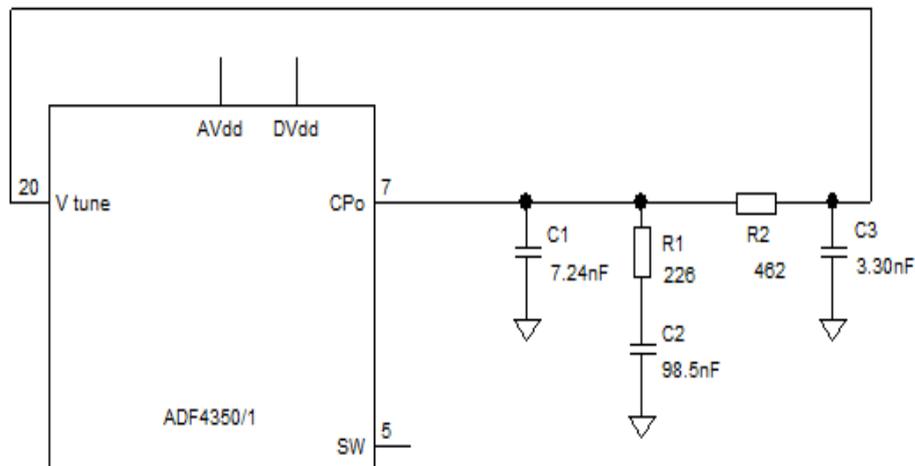


Fig.2. Parameters of loop filter

4MHz IF noise signal Generation

Based on the design, the noise signal source is not highly demanding. After be amplified and filtered, the IF noise signal can be generated from the base noise.

The amplitude of base noise is about -100dBm. In order to get the intermediate frequency signal which is suitable for mixing, the amplification of the base noise is necessary. In this design, The amplitude of IF signal is set to -30dBm. Therefore, the amplifier MAR-6SM+ by MINI's company is used, which is 21dB gain and 5V power supply. So this design has taken four stages of amplification. Circuit diagram of amplifier is shown in Fig.3:

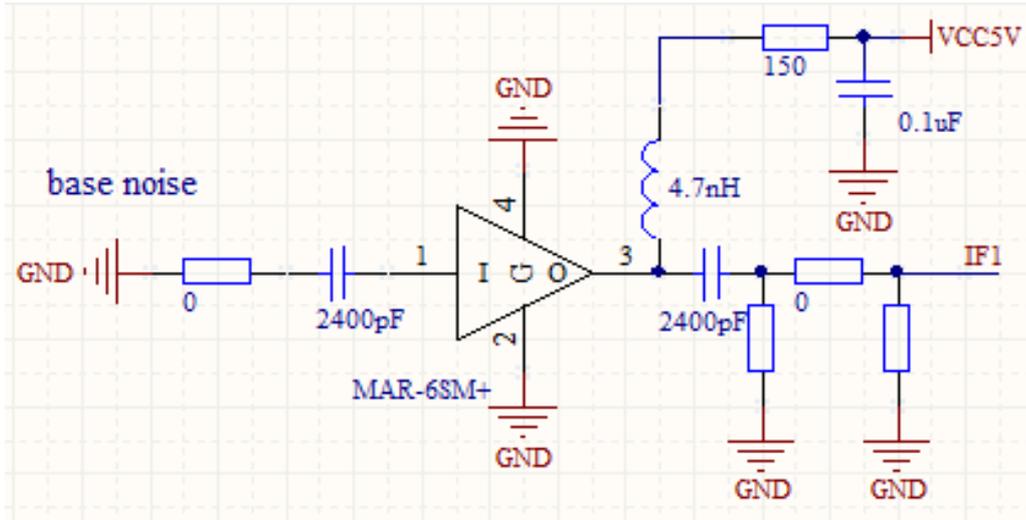


Fig.3. IF signal amplifying circuit

For the 4M broad-band IF signal, this design takes an SAW filter TB0564A by TST's company to filter base noise, of which the center frequency is 400MHz, bandwidth is 4M, and the insertion loss is 7.5dB. What's more, the test shows that SAW-TB0564A has good filter performance and meets requirements of jamming signal source.

Mixer design

Mixer is the key of the signal source. What's more, the selection of frequency of LO and IF have a great impact on the performance of output RF signal[9]. So this design takes the chip MAX2671 by MAXIM's company, which the range frequency of input IF is 40~500MHz, input LO is 600~2500MHz, and output RF is 400~4000MHz.

According to the principle of signal mixing, the frequency of LO and IF should be selected to avoid the AC signals in the target range of band frequency [10][11][12]. Based on the formula of signal mixing as Eq. (3):

$$RF = mIF \pm nLO \quad (3)$$

Where: m or n is an arbitrary integer.

Based on this design, signals are selected as $LO = 1975MHz, IF = (398 \sim 402)MHz$. Then Using APPCAD to verify all kinds of AC signals. The result is shown in Fig.4:

RF Freq. low	RF Freq. high	m	n
1,182.0	1,184.7	-3	2
786.5	788.6	-2	1
1,773.0	1,777.1	-2	2
1,572.9	1,577.1	-1	1
1,186.5	1,188.6	2	-1
1,448.6	1,451.4	3	-2

Fig.4. The result of simulation about AC signal

Based on the Fig.4, when $m = -1$ and $n = 1$, the output RF signal = 1573~1577MHz. And there are no AC signals to fall into the target range of band frequency. Therefore, the section of frequency of IF and LO and mixer chip MAX2671 meet the design requirements.

Hardware realization and RF test

The PCB is designed by Altium Designer, and four board structure. TOP layer and BOTTOM layer are for wiring lines, inner layers are for POWER and GND. Plate thickness is 2.0mm. The plate material is FR-4, and the dielectric constant is 4.60. The impedance matching is 50 ohm, and the design should be satisfied with the impedance matching principle. Between the different signal modules, deposited copper and external shield should be added to Shield interference. The PCB plate is shown in Fig.5:

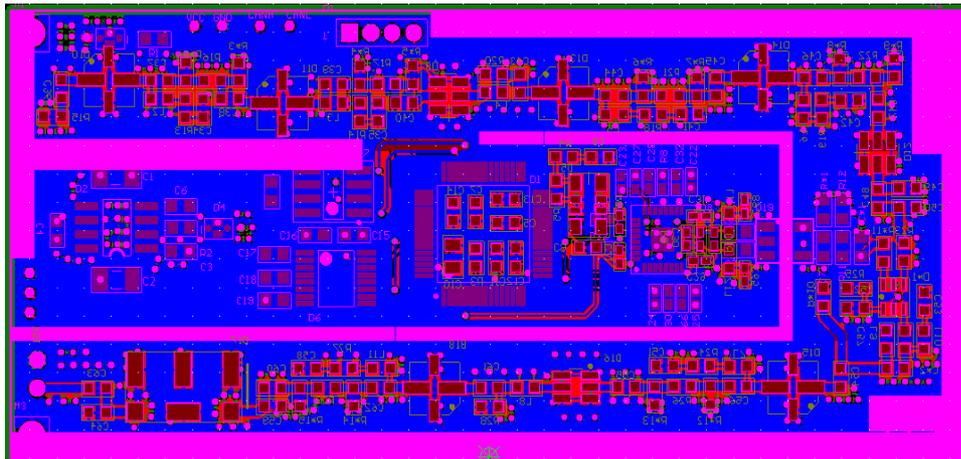


Fig.5. PCB of jamming source

Using Agilent spectrum analyzer E4408B to test the output RF jamming signal, the result is shown in Fig.6:

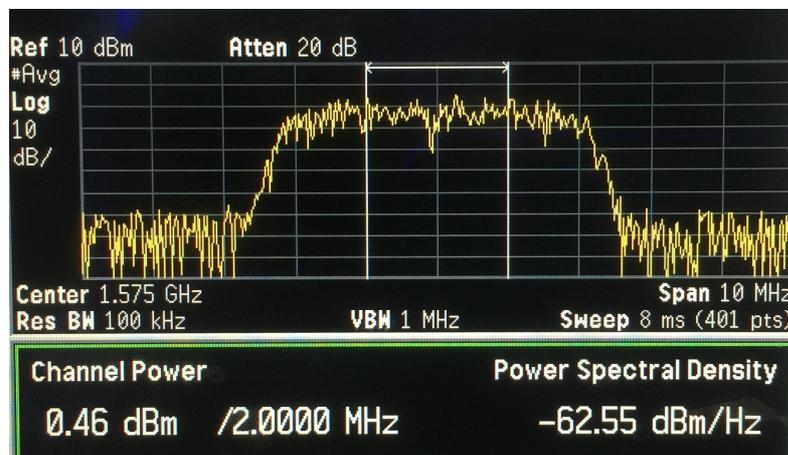


Fig. 6 Spectrum map of output broad-band jamming signal

According to the Fig.6, the output RF signal bandwidth is about 4MHz. The power of it is about 0dBm. And the performance of signal is stable and satisfied.

conclusion

This paper propose the design of broad-band jamming signal source for GPS-L1, which is based on signal generator ADF4351 producing LO signal and base noise producing IF signal. Furthermore, the central frequency and power of output RF jamming signal can be programmed control. And the actual test shows that the performance of the jamming source is stable and has a good interference effect on GPS.

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