Design of SAS real-time image display based on FPGA and DSP

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Abstract. In order to improve the performance of real-time, stability and high-resolution display of sonar signal processing system, the article designs and realizes a kind of mobile phone screen real-time display system based on FPGA + DSP, with The FPGA, DSP and SSD2828 device as the hardware core. It fully meets the requirements of SAS real-time processing system for display in the sonar image display system controlling, data transmission capacity and computing power with a combination of hardware and software.

1 Introduction

Synthetic Aperture Sonar [1] (SAS) is a kind of the new high resolution imaging Sonar system, which works does not depend on frequency and distance. Its basic principle is to use small-sized arrays along the virtual space of uniform linear motion to large aperture arrays. SAS transmits and receives echo signals orderly in the position trajectory, and conducts the echo signal with coherently overlap processing according to the different spatial positions and phase relationships, so as to form an equivalent large-aperture and high resolution obtained in the direction of movement. With the rapid development of FPGA technology, it is widely used in high-speed real-time signal processing with the characteristics of abundant logic resources, reprogrammable, flexible and fast integration of a variety of peripheral interface circuit. DSP has a sequential operation speed, complex computing power characteristics. The use of the system architecture of FPGA + DSP [2], sonar signal processing can have a very high performance of display and computing, and excellent flexibility and real-time. In this paper, it uses 1280*720 phone screen for display with the MIPI interface, which has high resolution and preferable images showing.

2 System Design

The hardware structure of the platform is based on FPGA + DSP. Wherein, FPGA uses Altera’s cyclone 4 series EP4CE15F17C8N with its clock rate up to 400MHz, and DSP adopts TI's TMS320F28335, its clock rate up to 150MHz. Figure 1 shows a block diagram of the hardware platform. As can be seen from it, the platform contains two parts: one is the control core with the DSP and its peripheral circuit, the other is the sonar image display core section with the FPGA and SSD2828, including FPGA and their peripheral circuits [3].

In the system, DSP mainly completes receiving operation data and interpolation algorithm. Then it stores in the SRAM via XINTF interfaces and transmits the data to FPGA. FPGA mainly completes the data Validation, and control the SSD2828 chip displayed the data on the phone screen.

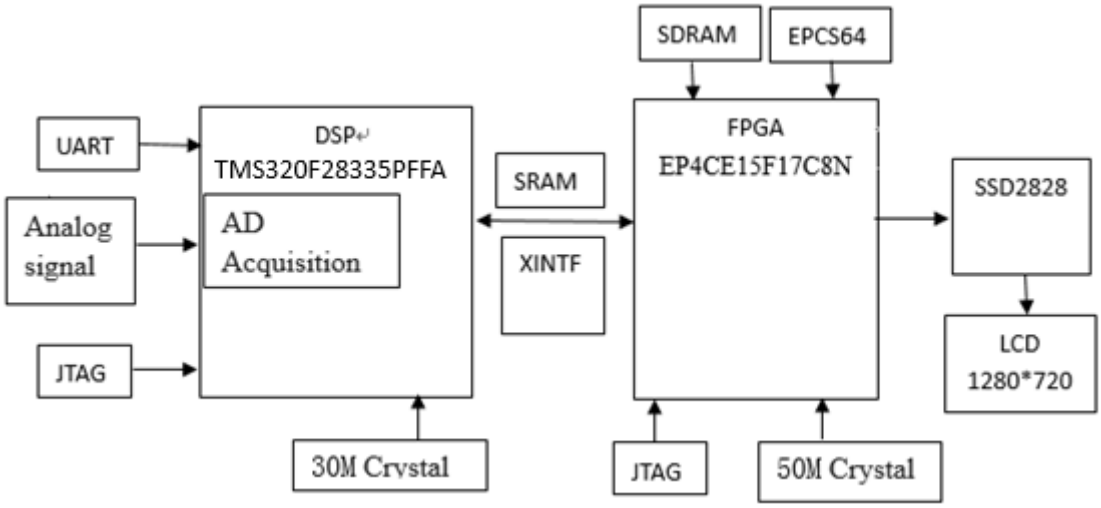

Fig. 1 System block diagram

3 Hardware circuit design

3.1 XINTF interface design

DSP writes data to the FPGA with the interface of XINTF and FPGA needs the internal RAM as the data buffer. There are 19 address lines and 16 data lines for data exchange. The SRAM pins are connected to the interface and the DSP XINTF pins on the FPGA. When data is written, DSP via low powered pin to inform FPGA to read data. If the DSP does not use the SRAM, FPGA can be used to dump the data to improve the speed of data reading and writing.

Provided in the FPGA is shown in Fig. 2. By two write buffers, and a high-speed read and write data FIFO [4].

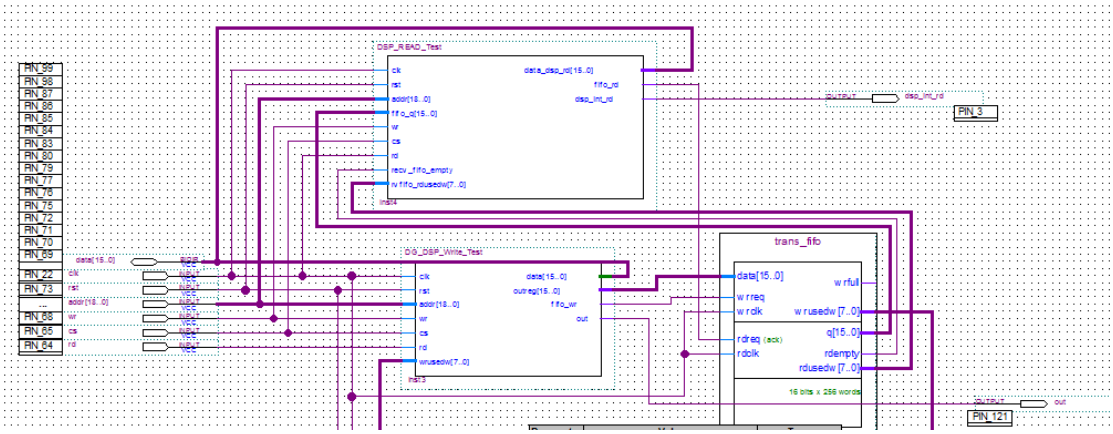

Fig. 2 FPGA internal design

3.2 SSD2828 interface circuit design

In the FPGA, the reading data is RGB format and required to be transformed into 4-channel differential signal by SSD2828 chip, and then displayed on the LCD via the MIPI interface.

As shown in Fig. 3, the clock is configured by the PLL in FPGA, the reset signal shared with FPGA, and the data is 16 bits wide.

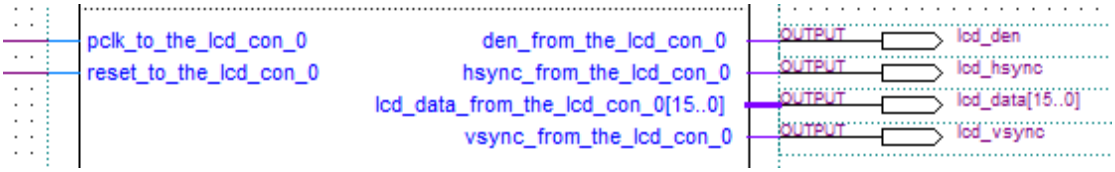

Fig. 3 SSD2828 interface design

4 Image interpolation algorithm

The sonar image is fan-shaped, and each image consists of 167 the echo signal lines. Each line collects 675 equally spaced points as sampling points. So the image signal acquisition system uses 167 * 675 specifications, and then transforms into 1280 * 720 image formats with the R-Theta interpolation algorithm [5].

Let the image of 167 lines in equal increments $\Delta\theta$ foot evenly distributed, four nearest sampling points and the plane Z adjacent pixel points is: $t_{i,j}, t_{i,j+1}, t_{i+1,j+1}$, Z_i, Z_{i+1}, which are the same corresponding points on the arc respectively. As shown in Fig. 4:

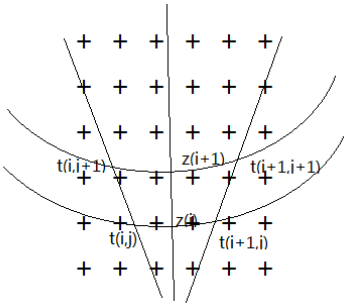

Fig. 4 R-Theta Algorithm

Since the image is displayed as 150 ° fan-shaped, $\Delta\theta$ and ΔR can be calculated as:

$$\Delta\theta = \frac{150\pi}{180*166} \approx 0.01576° \quad \Delta R = \frac{675}{765} = 1 \tag{1}$$

The adjacent two lines of echo signals are available interpolation calculation equation:

$$Z(i) = t_{i,j} * Reer + t_{i,j+1} * (1 - \theta err) \tag{2}$$

$$Z(i+1) = t_{i+1,j} * Reer + t_{i+1,j+1} * (1 - \theta err) \tag{3}$$

$Reer$ and θerr are the distance and angle relative error of radial and azimuthal respectively:

$$Reer = \left|r - \sqrt{x^2 + y^2}\right| / \Delta R \tag{4}$$

$$\theta err = \left|\theta - atctan\left(\frac{y}{x}\right)\right| / \Delta\theta \tag{5}$$

5 Result

We collect live signal stored in an array inside, and then read through the SCI of DSP. The DSP completes the interpolation operation and transmit it to the FPGA via the XINTF interface for display. Fig. 5 shows the actual effect:

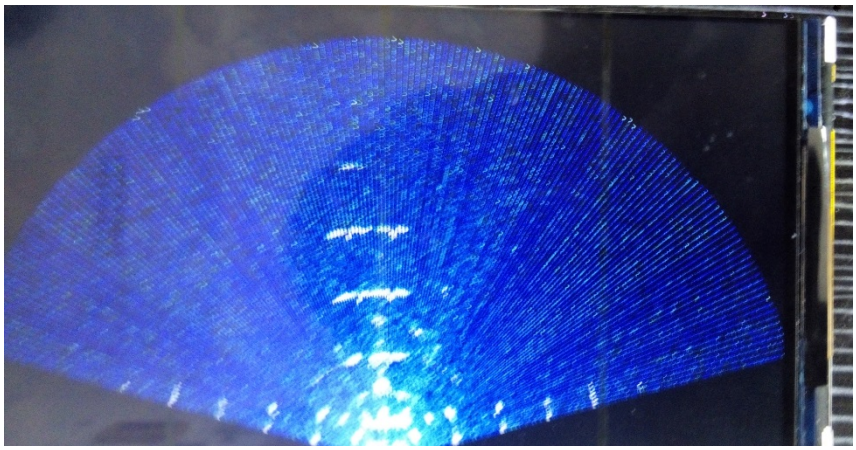

Fig. 5 image displaying

6 Summary

This article describes the conduct of high speed data transfer between the DSP and the FPGA, describes the hardware circuit design of FPGA and the image interpolation algorithm, and displays on the

phone screen. The system processing time is short, real good and meets the needs of SAS real-time image display.

References

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