4~6GHz 6-bit MMIC Digital Attenuator With Low Phase Shift

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Abstract. This paper presents the 4~6GHz 6-bit MMIC digital attenuator with low phase shift. Phase compensation techniques were used in the MMIC design to reduce the phase shift. This attenuator is fabricated with 0.25μm GaAs PHEMT process. Simulation results of the developed MMIC chips in the 4~6GHz show that the 6-bit MMIC digital attenuator has 0.5dB resolution and 31.5dB dynamic attenuation range, input return losses was less than 15dB and output return losses was less than 17dB for all attenuation states, RMS is less than 0.4dB; insertion loss is less than 2.4dB; phase shift error is less than 3° for 35 attenuation states.

1. Introduction

With the development of communication technology. Communication products are developing at many directions such as miniaturization、low-power and reliability. Due to its small size, good stability, capability, consistency and cheap in mass yield, Monolithic Microwave Integrated Circuit (MMIC) is becoming more and more important in the communication market.

MMIC variable attenuators are required in many satellite communication systems such as broadband communications, microwave radio communications, military radar, space communications and other electronic equipments. to control the signal level and adjust the system power budget. An attenuator specially is a key device of the module used in BFN because the attenuator is to control of the amplitude[1~2].

The attenuator has two types of control method, analog attenuator and digital attenuator. Digital attenuators offer better linearity, high power handling, and easy and accurate control of attenuation, So MMIC digital attenuators have gained lots of interest in recent years.

The requirements of the MMIC digital attenuators to be designed are as following: small size, high attenuation accuracy, low insertion phase shift, high reliability and low cost.

In this paper, we describes an MMIC digital attenuator with low phase shift in 4~6GHz. The 6-bit digital attenuator has obtained excellent performances and implements in GaAs pHEMT MMIC[3].

2. Circuit Design

Published literature on MMIC digital attenuators mainly rely on three basic types of topologies: i) Tee attenuator; ii) Bridged-Tee attenuator; iii)Pi attenuator. All of them relay on a signal through either a bypass line or an attenuation cell with RF switches[4].

Fig.1, Fig.2 and Fig.3 show the topologies of Tee attenuator, Bridged-Tee attenuator and Pi attenuator.

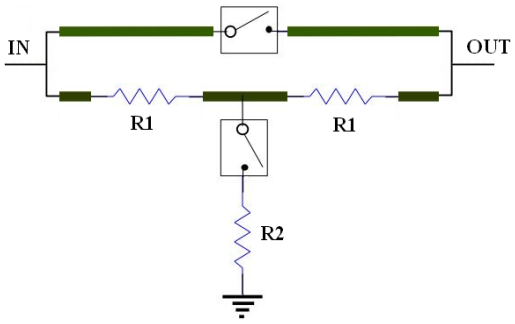

Fig.1 Tee attenuator

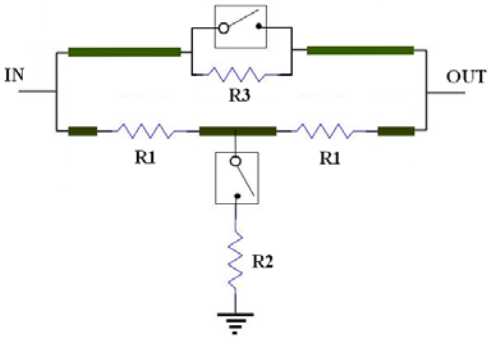

Fig.2 Bridged-Tee attenuator

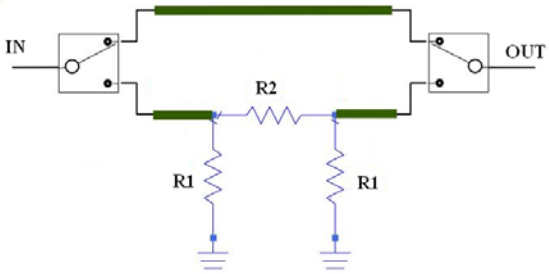

Fig. 3 Pi attenuator

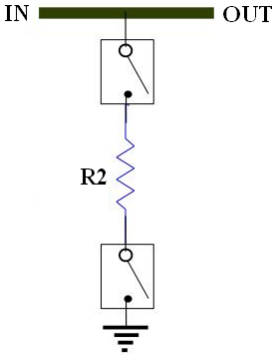

Fig.4 Simple Tee attenuator

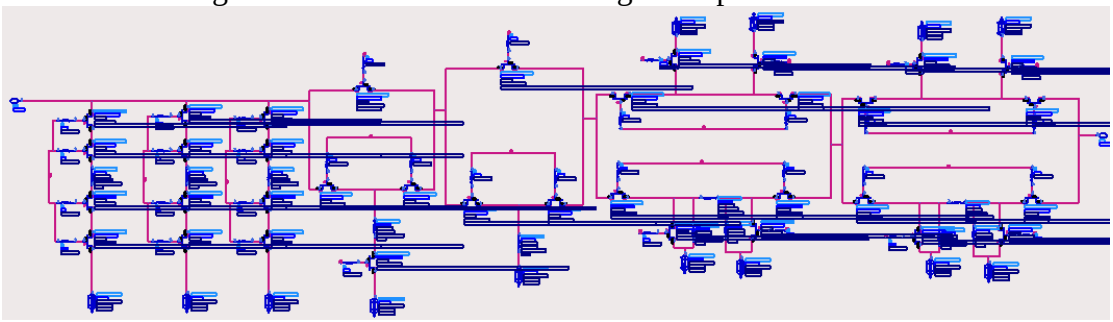

Fig.5 Schematic of the digital attenuator

Referring to FIG.5. the schematic of the 4~6GHz MMIC digital attenuator with low phase shift is shown. To achieve good performance, the circuit configuration as well as the process conditions, should be selected properly.

The digital attenuator consists of switched pHEMTs, capacitors, resistors, and microstrip lines. The switched PHEMTs in the circuit are controlled through 8kΩ resistors of the gate poles, which provide enough radio frequency isolation between the gate of each switched PHEMT and the control sources. And the low value resistors are used to form the topologies for attenuators.

The five required attenuation bits are the 0.5dB, 1dB, 2dB, 4dB, 8dB, 16dB providing a dynamic range from 0.5dB to 31.5dB. Tee attenuator (Fig.1) is selected for 0.5dB-bit, 1dB-bit, 2dB-bit and 4dB-bit attenuator,, Tee attenuator is chosen because of its good performance in insertion loss, input/output VSWR and has better attenuate precision than other. The Tee attenuator used in 0.5dB-bit and 1dB-bit is Simple Tee attenuator(Fig.4), compare to typical Tee attenuator, the Simple Tee attenuator without R1 and parallel pHEMT switch, the attenuator cell is represented only by R2 to the ground. The Tee attenuator used in 2dB-bit neglect the R1, microstrip lines lengths are used to have no phase shift between the two states. The 4dB-bit and 8dB-bit is acquired by using Pi attenuator (Fig.3), because of two switches, Pi attenuator has more insertion loss, but Pi attenuator is robust to the temperature variation and process. In perfect case, microstrip lines lengths between ON and OFF states is zero, In reality, Lengths are also used to have no phase shift between the two states, and use the same configuration in two channel[5~7].

The digital attenuator integrated driver was realized by enhancement /depletion (E/D)technology on GaAs substrate. The digital portion adopts a direct coupled FET logic (DCFL) structure， which

had the advantages of simple structure，high speed，low power consumption．simplify the system application and enhances the system reliability．The digital attenuator has built-in 5 voltage control port transistor-transistor logic (TTL) driving circuit to feed the pHEMTs' gate poles. In this case, when the control voltages are set at 0V, which is the negative pinch-off voltage of switched pHEMT, the switched pHEMT will work at its "off" state (high resistance). When the control voltages are set at 5V, The switched pHEMT will work at its "on" state. So the required attenuation can be obtained by switching the control voltages at the port.

The digital attenuator is at the minimum attenuation state, when all of the five control voltages are 5 V. In this case, the attenuator has a minimum insertion loss. The attenuator is at the maximum attenuation state, when all of the five control voltages are 0 V.

The above description is equally available for the other states. The control signal with the value of 0 V is taken as "0" and the control signal with the value of 5 V is taken as "1." The truth table of the digitally-controlled main attenuation states shows in Table 1, which is referred to in Fig. 5.

Table1 Truth table of main attenuation states shows ("1"as 0V, "0"AS -5V)

	0.5dB	1dB	2dB	4dB	8dB	16dB
	P1	P2	P3	P4	P5	P6
IL	1	1	1	1	1	1
0.5dB	0	1	1	1	1	1
1 dB	1	0	1	1	1	1
2 dB	1	1	0	1	1	1
4 dB	1	1	1	0	1	1
8 dB	1	1	1	1	0	1
16dB	1	1	1	1	1	0
MAX	0	0	0	0	0	0

Using the new configuration, a digital attenuator has been realized by GaAs process. The simulation of our digital attenuator have been presented based on the ADS2008. Broadband and low phase shift performance was achieved by optimization of the transmission line parameters and the resistor values.

The Monte Carlo analysis were also utilized in the attenuator design, the results predicted that the design has stability against the process variations.

3. Simulation Results

Using the new configuration, a digital attenuator has been realized by 0.25um GaAs E/D process. The simulation of our digital attenuator have been presented based on the ADS2008.Broadband and high precision performance was achieved by optimization of the transmission line parameters and the resistor values. The Monte Carlo analysis were also utilized in the attenuator design, the results predicted that the design has stability against the process variations.

The insertion loss is shown in Fig.6. The attenuator achieved a minimum insertion loss of 2.2~2.4dB in the entire 4~6GHz band. Referring to Fig.7, It can be seen that each curve in the figure represents a different attenuation setting in a roughly 0.5dB step with over 31.5dB dynamic range, for which a proper combination of the control voltages was chosen. Fig.8 and Fig.9 show the input return loss was always less than 15dB and the output return loss was always less than 17dB at any attenuation setting from 4~6GHz. RMS amplitude error was below 0.4dB. Fig.10 show difference between max and min phase shift for all values of attenuation, the value is less than 3° for 35 attenuation states.

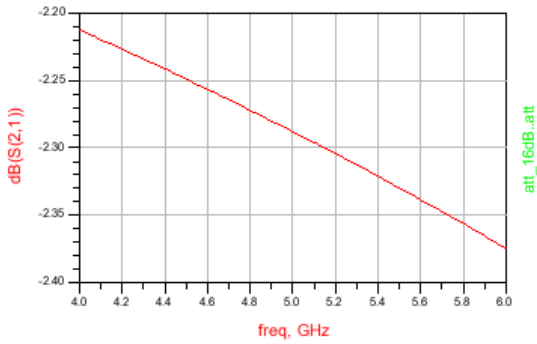

Fig.6 Insertion Loss

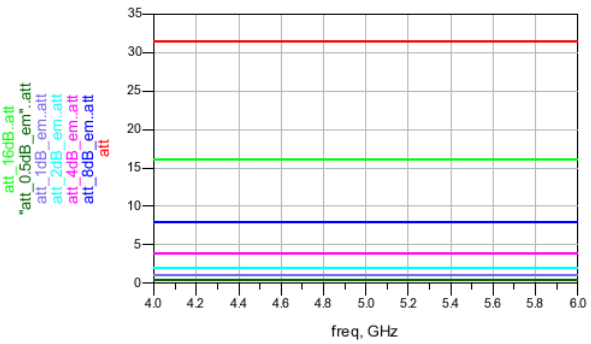

Fig.7 Relative Attenuation

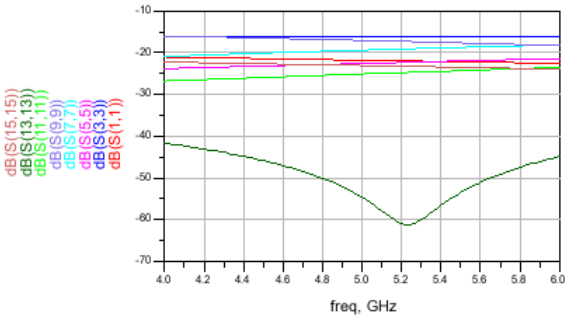

Fig.8 Input Return Loss

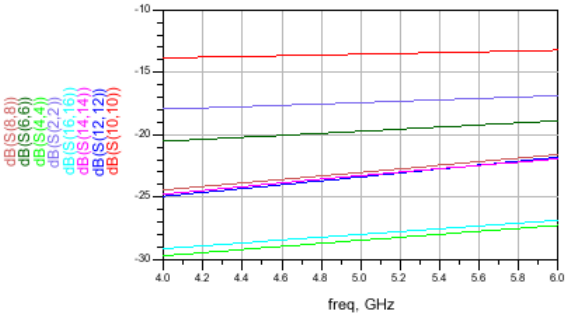

Fig.9 Output Return Loss

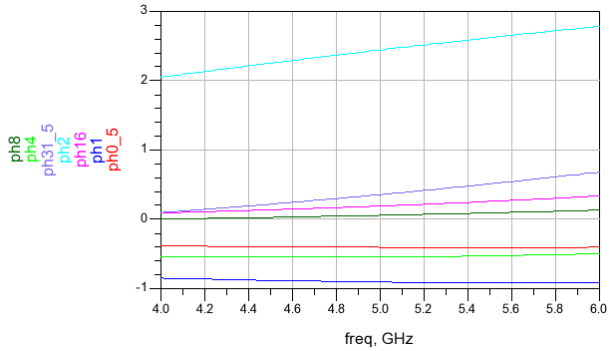

Fig.10 Relative Phase Shift

4. Conclusion

The theory, design, and measurement of a the 4~6GHz 6-bit MMIC digital attenuator with low phase shift are presented. Phase compensation techniques were used in the MMIC design to reduce the phase shift. To ensure high yield, Performance redundancy optimization strategy is used in design. the results of the developed MMIC chips in the 4~6GHz show that the 6-bit MMIC digital attenuator has 0.5dB resolution and 31.5dB dynamic attenuation range, input return losses was less than 15dB and output return losses was less than 17dB for all attenuation states, RMS is less than 0.4dB; insertion loss is less than 2.4dB; phase shift error is less than 3° for 35 attenuation states. This proposed MMIC has shown excellent performance covering 4~6GHz for digital attenuator.

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