Realization Of Vision Acquisition Module Based On STM32+OV7670 For Tunnel Robot

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Abstract. urban power conveying at present most of the use of underground channel and tunnel laying cable transmission, in order to ensure the power transmission of real-time, stability and continuity, we developed a robot tunnel for real-time monitoring of cable tunnel. This paper introduces a hardware solution of image acquisition based on single chip (OV7670), which can help the robot to realize the function of image monitoring and navigation.

1. Introduction to OV7670

OV7670 is a monolithic VGA camera and image processor features an image sensor that contains a 656*488 image array. It can output the whole frame, sub sampling, and other ways to take a variety of resolution 8/10 image data. Support for a variety of data formats, RGB RAWRGB (RGB 422, RGB565/555/444) and YCbCr (4:2:2), etc.. Its small size, low operating voltage, with a single chip VGA camera image processor function, the image can be gamma curve, white balance, saturation, color, etc.. After sensing the original image of the original signal, will be sent into the analog processor for processing, divided into G and BR channel into a A/D converter, converted into digital signals into the processor for further processing. The user can switch the graphics data sent by the test pattern generator by setting the relevant register. The processor module controls the whole process from the original signal to the RGB signal, and controls the quality of the image, including the edge enhancement, color space conversion, GAMMA control and so on.

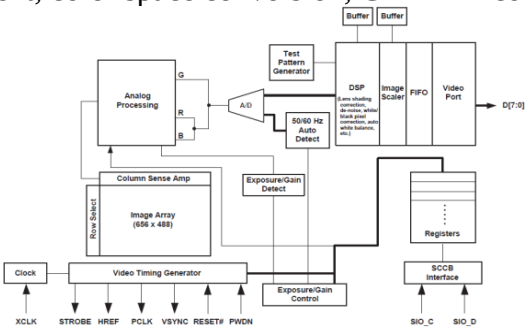

Fig. 1 OV7670 principle block diagram

2. System design block diagram

Design of the main design thought: the design of principle as shown in Figure 2: the STM32 micro control external IO mouth simulation sscb control bus (SCCB bus full name as the serial camera control bus, it works with the IIC is very similar to, is by definition of OV 3 wire serial camera control total line, can control most of the OV series image sensor), the ov7670 image sensing chip, an external image signal is transformed into rgb565 digital signal, data through FIFO, by STM32 control each frame image transmission. This paper mainly discusses from the FIFO to the image sensor to the data acquisition part, as well as the STM32 control program.

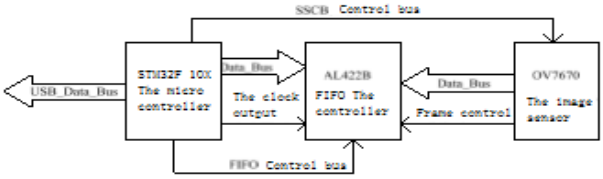

Fig.2 System design block diagram

2.1 Hardware Design

The main design points of this design is to achieve FIFO write control, design principle diagram of Figure 3 shows: in the design of FIFO FIFO_WEn and href as inputs to the NAND gate, and the output of the NAND gate received FIFO we port, only when the FIFO FIFO_WEn href for high power usually output to a low level. When the camera's HREF is high, FIFO_WEn is low, when the pixel data will be sent to FIFO. When HREF is low, FIFO_WEn usually does not send data into the FIFO high power, thereby preventing the acquisition of invalid data, the data through the P1 port into the STM32.

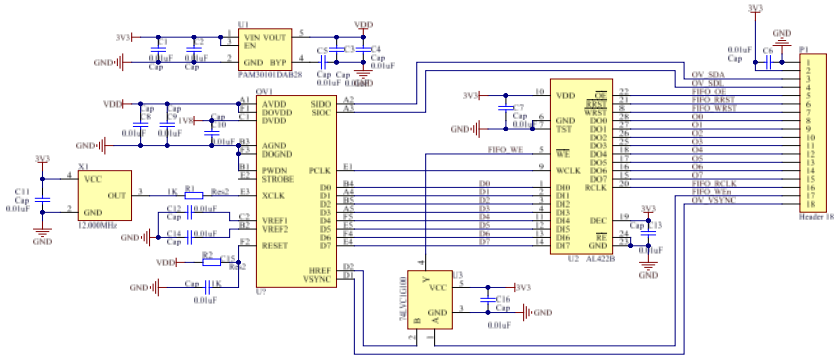

Fig.3 OV7670 image acquisition module based on the principle diagram

2.2 Software Design

STM32 no internal SCCB bus controller to achieve the control of the STM32 through the OV7670 module SCCB control bus timing. The basic process is shown in figure four:

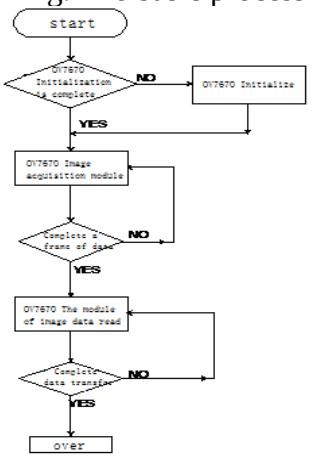

Fig.4 Flow chart of STM32 control program

SCCB control timing diagram is as follows:

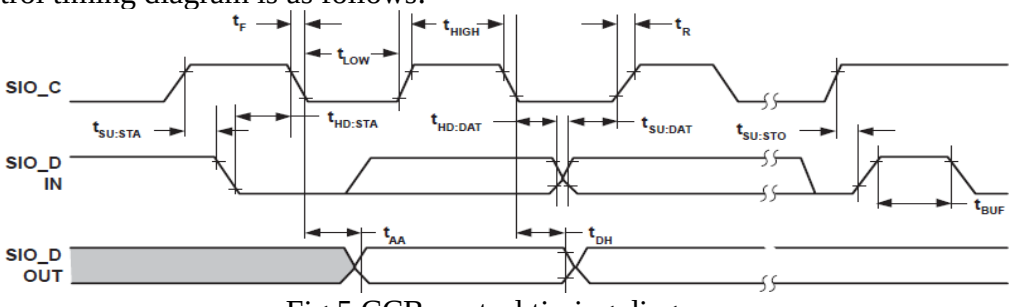

Fig.5 CCB control timing diagram

When the HREF is high, the camera data port with the pixel clock PCLK operation, has the output of a row of pixel data, when a line of data transfer is completed, HREF to a low level. At href for high level during, every PCLK output a basic unit of data and data in PCLK in rising along the stage to maintain stable. Therefore, main control chip configuration is interrupted should configured to rising edge interrupt, on the rising edge of the read data.

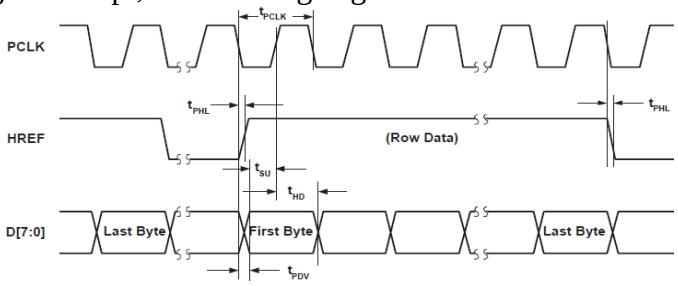

Fig.6 OV7670 line control timing diagram

OV7670_VSYNC mark, judge whether the FIFO receives an image. In the interrupt service routine, if the rising edge of the two VSYNC is detected (the image is received). Waiting for OV7670 frame synchronization signal (VSYNC), FIFO write pointer reset (FIFO_WRST=0), FIFO write enable (FIFO_WEN=1), wait for second frame synchronization signal (VSYNC), FIFO write inhibit (FIFO_WEN=0). VGA image frame sequence as shown in Figure: OV7670 frame output timing (VGA).

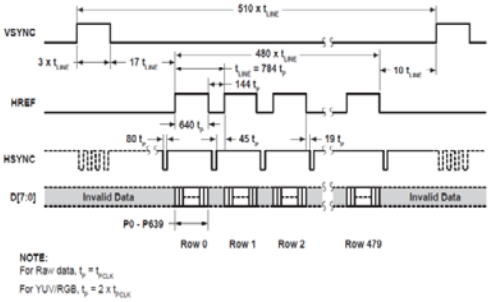

Fig.7 VGA image frame timing diagram

This design uses the RGB565 chip OV7670 pixel data output grid Type. The two byte representation of the red, green and blue components of a pixel, the pixel rgb565 format received image data, the output format as shown in the figure.

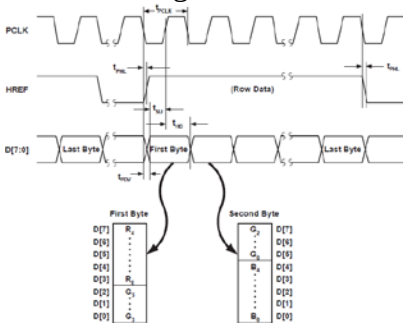

Fig.8 RGB565 image data format

3. Summary

This paper introduces a hardware solution for image acquisition based on single chip. Currently only considered several ideal condition, a feasible solution is discussed, also need to study it in practical application in the work environment may not long-term stable and reliable operation factors, also need to take corresponding measures to enhance the feasibility and stability of this scheme, to ensure the long-term reliable operation of the system.

Reference

[1] Image search and positioning system based on OV9653 and Image Search and Position System FPGA Based on 0V9653Camera Module and FPGA Livy Liu Xunsi (School of mechanical and electrical engineering and automation, Shanghai Univer, Shanghai 200072.

[2] Based on USB2.0 and FPGA image acquisition and storage system research, Dalian University of Technology, master's degree thesis Name: Zhang Tong The development of STM32 library practical guide [M] Liu Huoliang Yang Sen.