

Circuit design of Track-And-Hold Amplifier in Ultra-High-speed Folding-Interpolating ADC

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Abstract. Among the designs of ultra-high-speed analog to digital converter, folding-interpolating structure has great advantages in control of chip area and power dissipation. But the frequency-doubled effect of folding-interpolating ADC will restrict dynamic performances of ADC, such as bandwidth and linearity, etc. However, introducing Track-And-Hold Amplifier(THA) into folding-interpolating ADC can ease these shortages effectively, and thus improve dynamic performances of ADC. The structure of THA adopts open-loop structure, which could help realize the request of high speed without the influence of feedback circuit. To improve the circuit linearity, the input buffer adopts open-loop linearization technology and the output buffer adopts method of compensation and cancellation. Sampling switch also choose switch emitter follower sampling switch with greater dynamic performances. By introducing feed-through compensation capacitance, the input signal and hold signal can be completely separated, which could also help improve dynamic performances of circuit. Finally, the designed THA is taken a simulation with 3GHz clock frequency and 500MHz input frequency. The results of the simulation show that the THA can keep great dynamic performances even in ultra-high clock frequency, which lays solid foundation for further design of ultra-high-speed folding-interpolating ADC.

1 Introduction

Nowadays, the rapid development of telecommunication, radar technology and aerospace puts a higher request to the speed and bandwidth of Analog to Digital Converter(ADC). Ultra-high-speed ADC is widely needed in various fields. Folding-interpolating ADC not only can achieve the request of ultra-high-speed, but also has unique advantages in control of chip area and power dissipation. But the frequency-doubled effect of folding-interpolating ADC will restrict its dynamic performances of ADC. However, the introduction of THA can solve this problem. THA can not only solve the problem of limited bandwidth in ADC brought by frequency-doubled effect, it can also greatly improve the linearity of ADC. In a word, THA gives an effective solution to the poor dynamic performances of ultra-high-speed folding-interpolating ADC

This text first gives the structure of THA. And then, every part circuit of THA is introduced in detail. Afterwards, the overall circuit of designed THA is given. Finally, under the simulation to designed circuit, comparatively ideal results have been gotten.

2 Open-loop structure of THA

Because the goal THA is used in ultra-high-speed ADC, to reduce the influence of feedback circuit in sampling speed, open-loop structure^[1-4] shown in Fig.1 is adopted to realized ultra-high-speed request.

Without feedback circuit, the setting time of hold signal in holding capacitance C_H is only limited by input buffer and bandwidth of sampling switch. The working speed is apparently higher than the close-loop structure^[5] with feedback circuit.

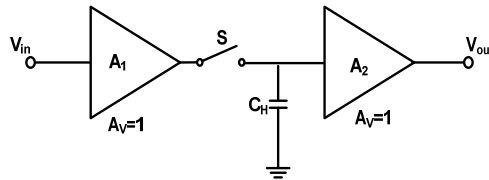


Fig.1 Open-loop THA structure

3 Specific circuit of THA

The constitution of THA shown in Fig.2 consists of input buffer, output buffer and sampling switch, etc.

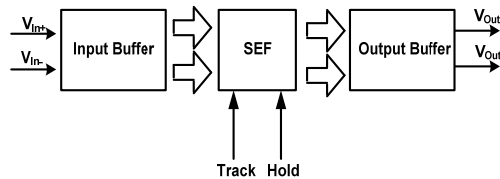


Fig.2 Structure diagram of THA

3.1 Circuit design of input buffer

Traditional differential input buffer^[6] with diode load exist problems of low linearity and limited voltage margin in ultra high frequency, which limits its application in high speed and high linearity THA circuit. To improve the linearity of THA, the high linear input buffer^[7,8] shown in Fig.3 is adopted. It consists of main amplifier, transconductance amplifier and auxiliary amplifier. Main amplifier and auxiliary amplifier adopt the same value emitter resistance R_1 , and the input ends of the two amplifiers are connected together. The transconductance amplifier is driven by output voltage of loads Q_3, Q_4 in auxiliary amplifier. Transconductance amplifier consists of Q_5, Q_6, R_2 . The equivalent transconductance is $G_m = 1/R_3$. Its output is connected with load R_3 of main amplifier. The value of load R_1 should be double of load R_3 to ensure that the output value of input buffer and input signal is the same. In this way, the output voltage of differential diode can be applied in the output nodes V_{out+} and V_{out-} of main amplifier. Nonlinear distortion can be reduced even without applying diode in main amplifier. To conclude, not only will the linearity of the circuit be improved by this open-loop linearization technology, but it also can achieve 1.2V wide-swing differential voltage input.

3.2 Circuit design of sampling switch

Currently, the diode bridge type sampling switch^[9] and the switch emitter follower sampling switch^[10-12] get widely application in designing high speed ADC. Not only is it difficult to finish the design of diode bridge type sampling switch, but the linearity of diode bridge type sampling switch is also worse than switch emitter follower sampling switch. So choosing switch emitter follower sampling switch will be better to improve the dynamic performances of THA. The detail circuit is shown in Fig.4.

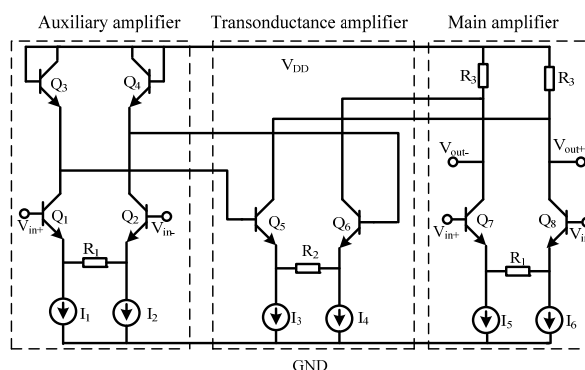


Fig.3 High linearity input buffer

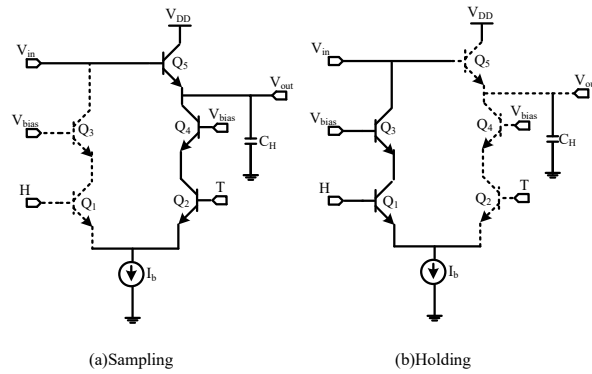


Fig.4 Switch emitter follower sampling switch

According to the basic characters of audion, switch emitter follower sampling switch (SEF) can eliminate charge injection following the changes of input signal. In the hold mode, switched-current I_b is controlled by transistors Q_1, Q_2 . When Q_1 is on and Q_5 is off, holding capacitance C_H keeps consistency of the voltage signal and sampling signal of last time. Transistors Q_3, Q_4 are used to reduce coupling clock signal of holding capacitance, so as to reduce clock feed-through.

3.3 Circuit design of output buffer

The function of output buffer is to separate the load of THA from holding capacitance, consequently offering enough driven capacity for THA to drive follow-up circuit, and reducing the influence to holding capacitance from the follow-up circuit. Fig.5 shows the output buffer circuit which adopts emitter deterioration structure. The shortages of traditional emitter deterioration structure amplifying circuit with only a couple of differential pair is current nonlinearity in collector caused by modulation effect of base voltage in Q_2, Q_3 . To compensate the nonlinearity caused by this reason, Q_1, Q_4, Q_5, Q_6, R_4 is added to outgoing end of emitter follower Q_2, Q_3 . By adjusting current and value of R_4 , making Q_2, Q_3 produces reverse current components to the components produced by modulation effect. Hence, the current produced by modulation effect is compensated. The linearity of the circuit can get further improvement^[13].

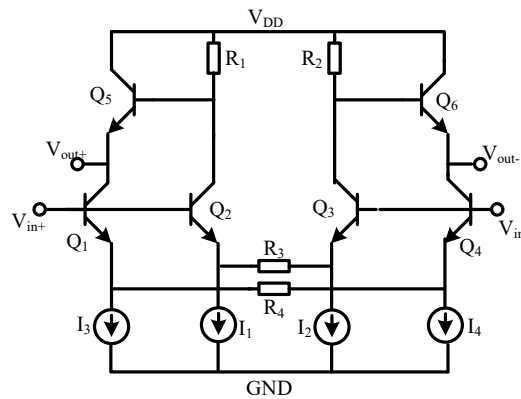


Fig.5 Output buffer

3.4 Circuit design of feed-through compensation

In the hold mode, the input signal and the holding capacitance C_H should be completely separated. However, in real situation, it can't be completely separated when sampling switch breaks away. To achieve the completely separation of input signal and holding capacitance, the feed-through compensation circuit shown in Fig.6 is introduced.

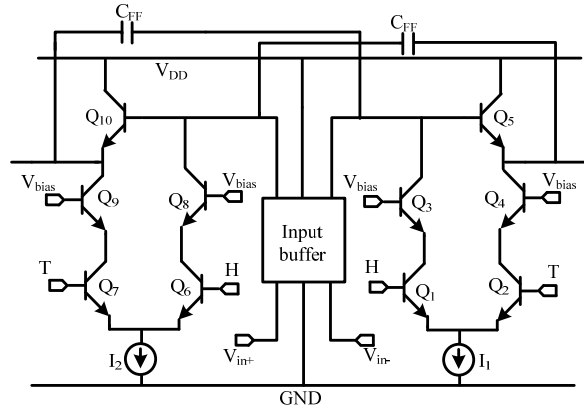


Fig.6 Feed-through compensation circuit

In the working condition of high frequency, the base-emitter junction capacitance of switch transistors Q_5, Q_{10} makes the holding capacitance feed through input signal. Although fully differential circuit can effectively weaken feed-through effect, the feed-through A_f still exists in the hold mode. The relationship between A_f , base-emitter junction of switch transistor C_{BE} and holding capacitance C_H is given by^[7]:

$$A_f = \frac{C_{BE}}{C_H + C_{BE}} \quad (1)$$

It can be seen that increasing C_H can reduce the feed-through in hold mode. But at the same time, the bandwidth of THA is also reduced. Therefore, the better way to reduce feed-through in hold mode is to introduce feed-through capacitance C_{FF} shown in Fig.6. The feed-through A_{fc} in hold mode becomes:

$$A_{fc} = \frac{C_{BE}}{C_H + C_{BE}} \left(1 - \frac{C_{FF}}{C_{BE}}\right) \quad (2)$$

When C_{FF} is equal to the base-emitter junction capacitance C_{BE} of switch transistor Q_5 or Q_{10} , the feed-through in hold mode can be completely eliminated, then the completely separation of input signal and holding capacitance can be realized.

4 THA circuit simulation

The overall circuit of THA is shown in Fig.7. The input buffer is what has been introduced in Fig.3. Besides, the feed-through capacitance C_{FF} ^[14] is realized by circuit shown in Fig.7. After choosing the component parameters as Tab.1 shows, the simulation to THA can be taken in software ADS2009U1.

Tab.1 Component parameters in circuit

Parameters	Value
V_{DD}	6V
$Q_1 \sim Q_4, Q_6 \sim Q_9, Q_{19} \sim Q_{26}$	Q1H151B1
$Q_5, Q_{10} \sim Q_{18}$	Q1H201B1
C_H	0.5pF
R_4	120.74Ω
R_3	134.08Ω
$I_1 \sim I_2$	3.59 mA
$I_3 \sim I_4$	3.68 mA
$I_5 \sim I_6$	3.62 mA
$I_7 \sim I_8$	3.71 mA

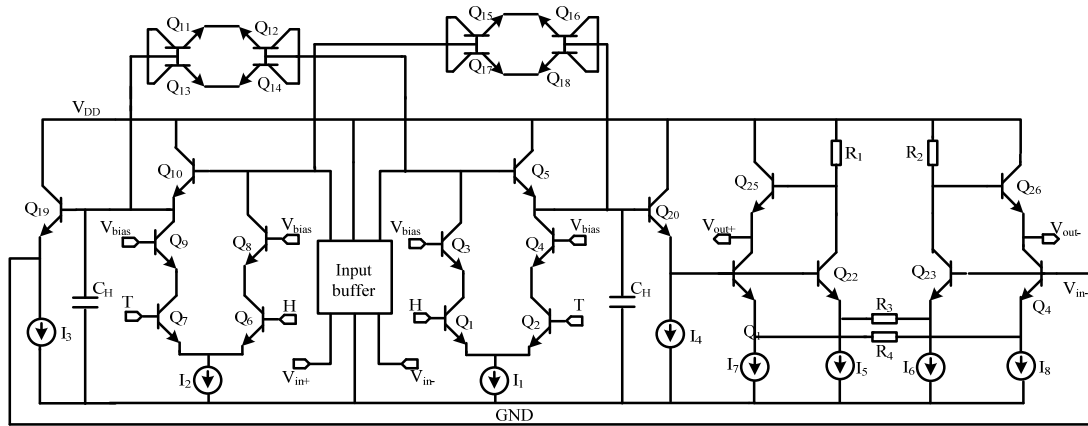


Fig.7 Overall circuit of THA

The designed THA is taken a simulation with 3GHz clock frequency and 1.2Vpp input signal range. The transient simulation result of THA output is shown in Fig.8. The voltage variety of output signal is about 2mV in hold mode. The hold time is about 125ps in reality, which is different to half of sampling wide 333ps. This is because it takes time to establish the hold mode after the hold mode instruction is given to the circuit.

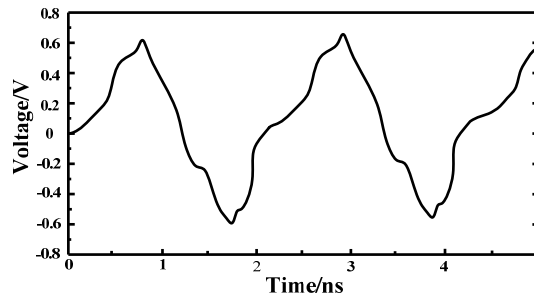


Fig.8 Transient simulation result of THA output

Fig.9 shows that at 3GHz sampling rate, the Effective Number Of Bits (ENOB) changing curve along with the changes of input signal. It can be seen that the ENOB can reach 8.74 bit at the situation of relatively low input frequency. The effective bandwidth ERBW can reach almost 900M.

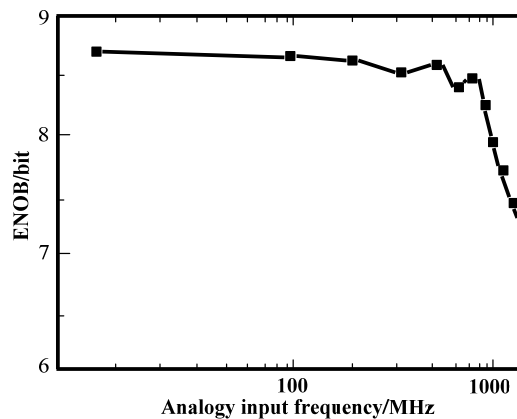


Fig.9 Effective Number Of Bits changing curve along with input signal

5 Summary

This text succeeds in finishing the circuit design of track-and-hold amplifier in ultra-high-speed folding-interpolating ADC. In addition, an effective solution to the poor dynamic performances of folding- interpolating ADC caused by frequency- doubled effect is provided, which can accelerate the development of ultra- high-speed folding-interpolating ADC. The simulation results show that, even in ultra high sampling rate, the designed THA can still keep good dynamic performances within the input bandwidth. It demonstrates the effectiveness of linear and bandwidth optimization in designing every part of THA.

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