A Circuit Design Based on high-speed serial communications data transfer network communication interface module

Fan Tiansuo, Hu Longtao, Zuo Dongguang, Li Fengchen, Zhou Bing , Chen hao

Xi'an Research Institute of High Technology, Xi'an 710025, China

523098802@qq.com

Keywords: Data Module;The power supply circuit; Communication Interface.

Abstract. Automation control and other consumer devices, industrial control and other fields, external communication interface many devices is still low speed serial port, but the low-speed serial inherent disadvantages: inability to concentrate, comprehensive, accurate and real-time monitoring data, which requires the design of serial communication data transfer network communication module; embedded system hardware design is the basis for successful design, and the design data module circuit basic circuit is the key to the success of the system hardware, the paper describes the hardware design of serial communication data transfer network communication module, and details the basic circuit design of the data module. the test results show that the basic circuit design fully meet the requirements of the system functions.

Introduction

In the field of automation and control, external communication interface many devices is still low speed serial ports. Thus, the disadvantages of the existing system are: inability to concentrate, comprehensive, accurate and real-time monitoring data. With the advent of Ethernet in the industrial, commercial areas of large-scale use of momentum and network automation, users and suppliers is an urgent need real-time access to data and can be controlled at any time and any place, so remote rapid failure analysis and processing , remote maintenance equipment, in order to improve quality, increase productivity and reduce overall costs. Completely replace these serial communication devices are neither economic nor feasible. This requires design data transfer module serial communication network communications. Embedded system hardware design is the basis for successful design, and the design of the data module circuit basic circuit is the key to the success of the system hardware.

Organization of the Text

The overall design of the system hardware overview

The main function of the serial communications data transfer network communication module is complete networked serial devices, and provides serial, Ethernet port and U SB port three download mode. According to the functional requirements, the hardware composition shown in Fig1.

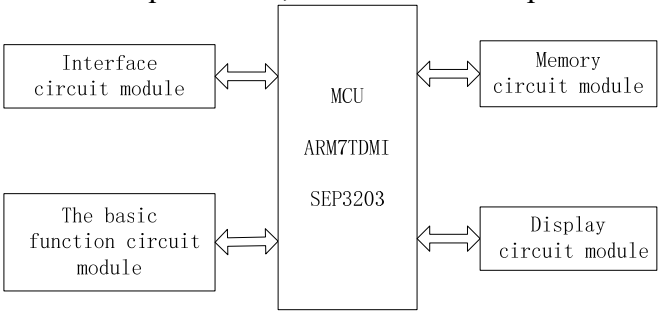

Fig.1 Frames turn serial communication network communications hardware modules

To achieve the study converter module, first choose a hardware platform that is embedded

processor. Because ARM is based on reduced instruction set (RISC) 32-bit core, high code efficiency, fast, strong overall performance in the ARM architecture-based embedded CPU, based on the SEP3203 ARM7TDMI embedded microprocessor architecture has a more good technical support, so this converter selection SEP3203 as the hardware platform; the same time, a system, the basic circuit is essential that the power supply circuit, a clock circuit, monitoring and watchdog circuit, JTAG circuit, a power supply circuit for the entire system to provide power to the system clock circuit to provide clock work, monitoring and watchdog circuit to ensure reliable operation of the entire system, JTAG circuit for the system debugging; because users need to have serial converter, USB and Ethernet port download capabilities and the baud rate of industrial equipment is generally from 2400 to 57600, so this converter to have a RS232 / 485 serial ports, USB and Ethernet interfaces; SEP3203 according to the start-up mode and program code storage requirements, data module must be present a memory, in order to meet the user's display function, a display function must be viewed by the user. The basic circuit design is the basis for the entire system design, the following describes the basic circuit design system.

The basic circuit design of system

The design of power supply circuit

The quality of the power supply circuit, a direct impact on the stability of applications, reliability, power consumption, cost, and battery life and reliability. First Mains AC220V get through ACDC module DC5V power supply, input power supply of the entire system; 5V ~ 3.3V LDO is the result of the converted, it to Garfield and other peripheral circuits require 3.3V power supply; 5V ~ 2.5V LDO is the converted, and R2 (10K) and C6 (10uF) composed of a delay circuit, the delay AMS1172.5 power supply Garfield core chip circuitry. For conversion chip LDO, the current from the power ripple system, stability and price considerations, we use the AMS1117 series, the input voltage of the chip is 3.0 ~ 12V, output current up to 800mA, AMS1117 can be adjusted to 1.5V, 1.8 V, 2.5V, 2.85V and several voltage 5V, 3.3V and 2.5 respectively by L DO voltage conversion chip AMS1117_3.3 and AM S1117 _ 2 5 composition obtained, the conversion circuit shown in Figure 2.

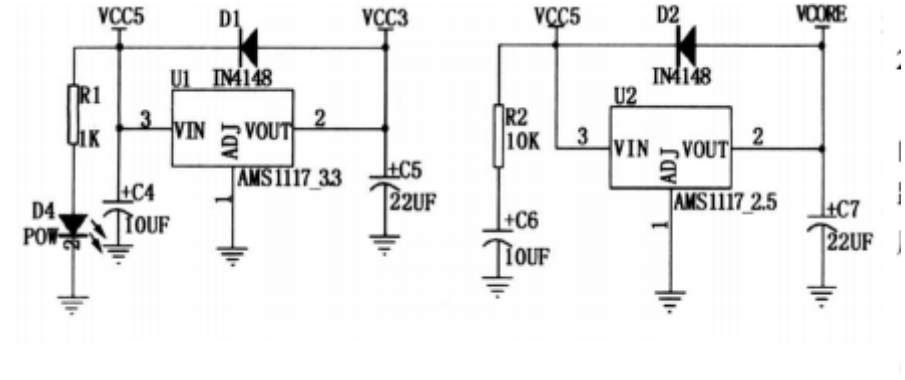

Fig.2 AMS1117(5V～3.3 V) and 5V～2.5V LDO circuit

The design of Clock circuit

Passive system uses 10MHz crystal to provide the master clock when the system is operating in Normal mode, the system clock generated by the CPU inside a PLL frequency multiplier circuit, can be up to 100MHz (typical operating frequency is 75MHz); through another PLL frequency multiplier circuit generate 48MHz clock, which supplied USB use; when the system is operating in Slow mode, the direct use of an external crystal oscillator as the system clock. By setting the PMC (Power Management Module) PMDR (mode register) corresponding bit system can enter Slow, Normal, Sleep, Idle mode.

RTC clock module system uses passive crystal 32.768kHz clock to provide real-time control module. In low-power mode and the system reset process, RTC module maintain normal work, to avoid the other operating result in the loss of the system clock. Typically, the crystal oscillation circuit schematic of FIG.3[4].

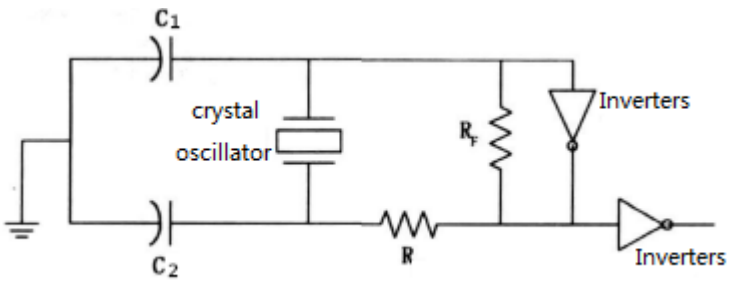

Fig.3 Crystal/ceramic oscillation circuit

In Figure 3, C1 is the phase adjusting capacitor; C2 for the gain adjustment capacitors; resistor RS is used to prevent excessive crystal drive. In the crystal oscillator, the resistance RF10M. Only high-speed crystal oscillator may only require Rs (100 <Rs <1k). C1 general frequency crystal oscillator circuit, C2 take 15pF.

According to the schematic above crystal oscillation circuit, the system clock circuit design shown in Figure 4. Since the PLL circuit chip of both frequency and signal amplification purification function, so the system can lower external clock signal to obtain a higher operating frequency, due to reduced clock speed switching caused by high-frequency noise.

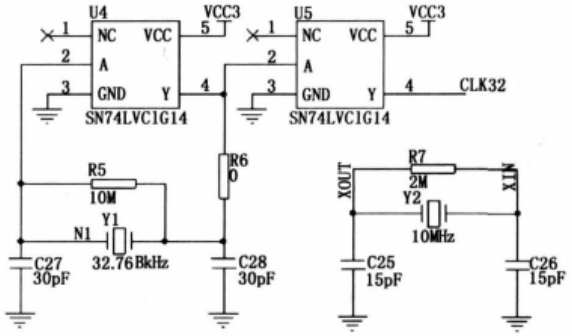

Fig.4 Clock circuit

The design of monitoring and watchdog reset circuit

This circuit is designed using Maxim has introduced the small size, low power consumption MAX823, it has a 5-pin up (microprocessor) supervisory circuits, and a watchdog input and manual input of the chip, the circuit shown in Figure 4.

Reset circuit monitor main function is the power supply voltage or below the set threshold generates a reset output to ensure that the microprocessor SEP3203 work at the power supply voltage, the system clock is stable and reliable conditions. In the circuit, when the supply voltage drops to a specified threshold value, RESET goes low, the MAX823 output low voltage reset pulse, reset control, after the power supply voltage restored, RESET goes high after a time delay . MR pin of MAX823 to manual reset input pin that allows the user or an external power supply system under normal conditions will reset the microprocessor, provides a convenient system testing, uninterrupted work is necessary for the system function. Watchdog manually reset the system C51 has delayed work to eliminate manual input jitter.

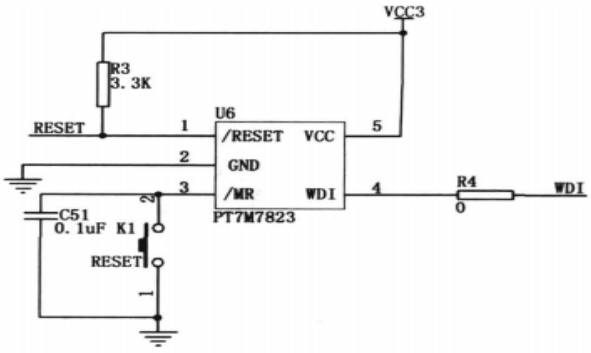

Fig.5 Reset and watchdog circuit monitoring

Watchdog Timer works: when the system is working, the impact of the software clock or other

factors will fall into an infinite loop, the watchdog timer ∀ WDI can detect pulses regularly sent microprocessor. If the trigger signal is not received within the specified time, then that system fails, the output is low, it will send an alarm signal and interrupts the microprocessor work. The watchdog output is connected to the output of the power supply monitor reset signal is generated when the system receives a reset command to stop WDI pin, the chip's RESET control system reset.

CPU software Under normal circumstances must be within a certain period of time to clear the watchdog dog operation, clearing the dog in many ways [5], we use the dog's task clear way to set a highest priority task and clear the dog, a minimum priority tasks accumulating counter. In the high-priority task of detecting counter at a certain time if there is an increase, if the counter is 0, then during this time, the lowest-priority task has not been run, indicating that certain tasks occur an infinite loop, you need to reset .

The design of JTAG interface circuit

Joint Test Action Group (Joint Test Action Group, JTAG) protocol is an international standard test, mainly used for chip testing and system simulation, debugging, JTAG embedded debugging technology is a technology, it inside the chip package special test circuit test access port (T est access port, TAP), through a dedicated TAG testing tools to test the internal nodes. Currently most of the more sophisticated devices support JT AG protocols such as ARM, DSP, FPGA devices, etc., SEP3203 chip also supports JTAG protocol. Standard JTAG interface is a 5 line: nTRST, TMS, TCK, TDI, TDO, were selected as a reset signal, the test mode, the test clock, test data input and test data output.

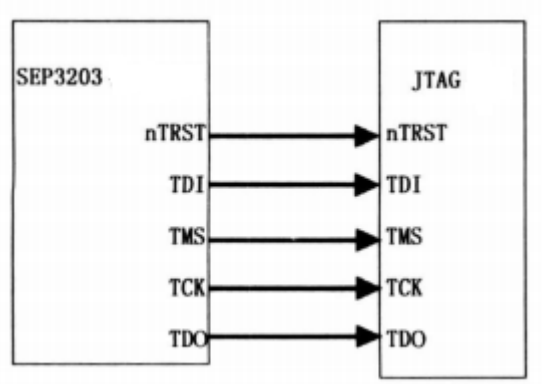

Fig6 JTAG debug connector with the connection diagram SEP3203

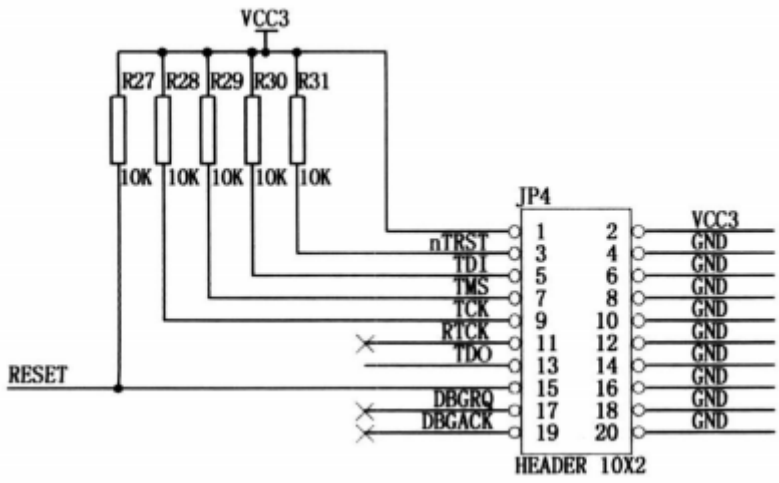

Fig.7 JTAG debug interface

JTAG testing allows multiple devices through the JTAG interface connected together in series to form a JTAG chain, to achieve the various devices were tested. JTAG interface also commonly used for in-system programming (In System Programmable, ISP) function, such as Flash devices programming. Through the JTAG interface, for all components within the chip access, so it is a simple and efficient means for developing and debugging embedded systems. Currently, JTAG connection interface, there are two criteria, namely 14-pin connector and 20-pin interface, our

system uses the 20-pin connector. Figure 6 is a JTAG interface and SEP3203 microprocessor system connection diagram. FIG. 7 is the actual JTAG circuit connection diagram.

Functional and performance testing

After the hardware design is completed, the data module debugging, and some of the data measured during the operation of the main module. With these data, the overall performance can have a general understanding.

Tab.1 The operating current and the operating voltage of microprocessor

	Operating Voltage(v)	Operating current(mA)
SEP3203 microprocessor	3.3,2.5	300

Tab.2 System Voltage Test Chart

	Theory value(v)	Actual measured value(v)	Deviation(v)
External output voltage	5	5.10	0.10
5V~3.3V LDO	3.3	3.45	0.15
5V~2.5V LDO	2.5	2.56	0.06

On the PC side running serial debugging assistant, the software is available free from the Internet, be set according to the actual operating environment to run the software. After testing, the module forwards the data properly.

Summary

At present, some equipment also uses traditional serial port (RS232) through

Letter, since these do not have the complete serial protocol specification, not a good judge of right and wrong packets, poor reliability during long-distance transmission, and can not access through IP Internet, and online monitoring. Therefore, the development of serial communication transfer network communication module has practical significance and socio-economic value. This module uses A RM processor as the core of the system, replacing the past low-grade CPU, embedded real-time operating system can be ported to the system hardware platform. Low CPU use of a single task structured programming, can not achieve real-time systems such requirements; embedded real-time operating system, multi-task programming, synchronization, mutual exclusion primitive operations without user programming between tasks to achieve.

RTOS task scheduling algorithm determines the execution order of tasks more enhanced real-time performance of this module. This paper introduces the basic circuit design data module, that is a power supply circuit, a clock circuit, monitoring and watchdog circuit, JT AG interface circuit design, the final test to verify the feasibility of the program.

References

[1] Wang Shuilian. Development of special purpose fuse testing system [D]. Harbin Institute Of Technology，2013.

[2] Ma Shaojie, Zhang He. Classification and correction strategy of fixed distance error for air blast Fuze [J]. Journal of Ballistics，2008，20(3):75-78.

[3] Wang Bing, RUAN Chaoyang. General Technology of System on Chip Based Programmable Fuze ESA Monitor[J]. Journal of Detection &Control，2013，35(3):61-64.

[4] Fang Shaojun，Li Guolin，Shang Yaling. General Design of the Control Circult for a Contact Airburst Fuze[J]. Journal of Detection & Control，2006, 28 (1): 21-24.

[5] Zhanwen XI,, Weirong NIE,, Qilei LI. A MEMS Interrupter Mechanism for Fuse Safety & Arming Device [J].International Conference on Mechanical Engineering and Mechanics, 2009, 3:51-56

[6] Wang Bing, Mo Jianjun. Knowledge Acquisition System Constructed by C++ Builder[J].JOURNAL OF SYSTEM SIMULATION， 2002, 14(10):1356-1358.

[7] Zhang Yajun，Zhang Jianjun，Qi Xihong，Cheng Linlin. Development of automatic detecting instrument for many kinds of fuse circuit board [J]. Mine Warfare & Ship Self-defence，2014，22 (2): 30-33.