Design and Simulation of Phase Locked Loop Circuit Based on VCO Optimization

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Abstract. This Paper stars from the basic working principle of PLL, obtains the mathematical model of PLL based on the traditional PLL structure, and analyzes the phase-locked loop tracking performance, acquisition performance, stability and noise performance, and other performances of PLL. This paper describes the overall PLL circuit and the phase frequency detector, loop filter, VCO, frequency divider and other circuit modules. In the analysis and design, we use MATLAB to do the simulation of the circuit. The PLL circuit has reached the design requirements.

Introduction

Phase-locked loop (PLL) is a closed-loop automatic control system which can track the phase of the input signal. It has been very widely used in all areas of radio technology. Initially, DeBellescize proposed the synchronous detection theory, and first published on the description of phase-locked loop in 1932, but it did not attract widespread attention. It is not until 1947 that the PLL was first be used in television receivers horizontal and vertical scanning synchronization. Since then, the PLL started to be applied.

The basic theory of PLL

The operational principle of PLL

As a system, PLL includes three basic modules: a phase detector, a low-pass filter which is the loop filter, and a voltage controlled oscillator. In this section, we firstly analyze the phase detector, loop filter and voltage-controlled oscillator.

Phase Detector

PLL phase detector (PD) is usually formed by an analog multiplier, and the PD circuit composed by analog multiplier is shown in Fig 2.1:

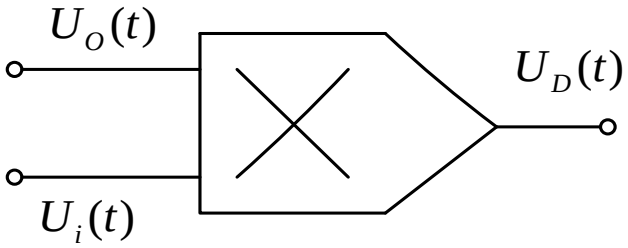

Fig2.1 The analog phase detector circuit

Let the signal voltage of external input and the signal voltage of controlled oscillator output to be:

$$u_i(t) = U_m \sin[\omega_i + \theta_i(t)] \quad (2.1)$$

$$u_o(t) = U_{om} \sin[\omega_o + \theta_o(t)] \quad (2.2)$$

Where ω_O is the oscillation angular frequency of the VCO when the input control voltage is zero or a DC voltage, and this frequency is called natural oscillation angular frequency. Then the output voltage of analog multiplier is:

$$U_D = Ku_i(t)u_o(t) = KU_mU_{om}\sin[\omega_i t + \theta_i(t)]\cos[\omega_o t + \theta_o(t)]$$

$$= \frac{1}{2}KU_mU_{om}\sin[\omega_i t + \theta_i(t) + \omega_o t + \theta_o t]$$

$$+ \frac{1}{2}KU_mU_{om}\sin\{[\omega_i t + \theta_i(t)] - [\omega_o t + \theta_o t]\} \quad (2.3)$$

The transmission characteristic of the phase detector is:

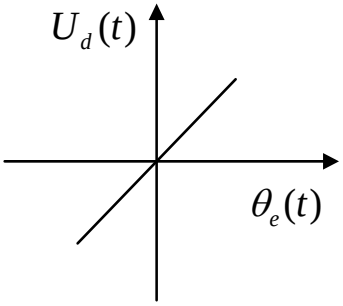

Fig 2.2 the transmission characteristic of the phase detector

Low-pass filter

Low-pass filter (LF) filters off the and frequency component in equation 2.3 above, and let the remaining difference frequency component be the input control voltage $U_c(t)$ of the VCO, which is :

$$uc(t) = \frac{1}{2}KU_mU_{om}\sin\{[\omega_i t + \theta_i(t)] - [\omega_o t + \theta_o t]\}$$

$$= U_{dm}\sin\{(\omega_i - \omega_o)t + [\theta_i(t) - \theta_o(t)]\} \quad (2.4)$$

Where ω_1 is the instantaneous oscillation angular frequency of the input signal, $\theta_1(t)$ and $\theta_2(t)$ is respectively the instantaneous phase of the input signal and the output signal, according to the relationship of the phasor we can get the relationship between instantaneous frequency and the instantaneous phase:

$$\omega(t) = \frac{d\theta(t)}{dt}$$

Which is

$$\theta(t) = \int \omega(t)dt + \theta_{do} \quad (2.5)$$

The instantaneous phase difference θ_d is

$$\theta_d = (\omega_i - \omega_o)t + \theta_i(t) - \theta_o(t) \quad (2.6)$$

Differentiating on both sides, we can obtain the equation of the frequency difference

$$\frac{d\theta_d}{dt} = \frac{d(\omega_i - \omega_o)}{dt} + \frac{d[\theta_i(t) - \theta_o(t)]}{dt} \quad (2.7)$$

Equation 2.7 above equals to zero, and the mathematical model is:

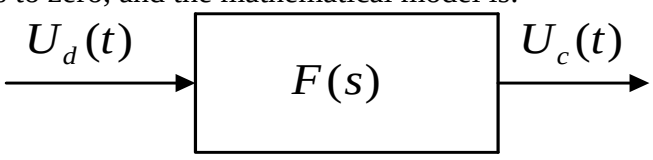

Fig 2.3 The model of the loop filter

Voltage-controlled oscillator

The voltage control characteristic of voltage-controlled oscillator (VCO) is shown in Fig 2.4:

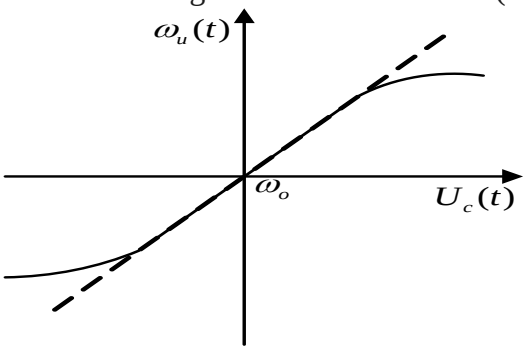

Fig 2.4 the voltage control characteristic of VCO

This characteristic shoes the oscillation frequency ω_u of the VCO varies linearly with the input signal voltage $U_c(t)$, and this relationship can be expressed as followed:

$$\omega_u(t) = \omega_o + K_o u_c(t) \qquad (2.8)$$

The above equation shows, when $U_c(t)$ changes with time, the oscillation frequency ω_u of Voltage-controlled oscillator (VCO) also changes with time, the PLL gets into the "frequency pulling", it tracks and captures the frequency of input signal frequency, and to let the PLL enters a locked state, and the state of $\omega_o = \omega_1$ remains unchanged.

The working condition of PLL

PLL has four operating states: locked state, out of lock state, capturing process and tracking process.

1. Locked state: the whole loop has reached the steady state of input signal phase. It refers to the phase of the output signal equals to the input signal phase, or there is a fixed phase difference between these two phases, but these two signals have the same frequency. In the locked state, the voltage control signal of VCO is close to flat.

2. Out of lock state: the difference of the frequency of the PLL feedback signal and the frequency of the loop input signal can't have the steady state of zero. When the design of the loop structural has problems, or when the input signal is beyond the application scope of the PLL, it will enter the out of lock state.

3. Capturing process: it is the process that the PLL enterS the locked state from the out of lock state. This status indicates that the loop has begun to enter the work, but has not yet reached steady state locked.

4. Tracking process: it is the process that the loop maintain the locked state through automatic adjustment, when the PLL has entered the locked state and the frequency or phase of the input signal changes for other reasons.

The simulation of second-order PLL loop

All the simulations use the second-order PLL loop. This is because most of the PLL we used in practical application are second order, or designed to approximate the second-order loop by ignoring the higher-order effects. In view of the practical application sense of the second-order PLL, in this simulation we use second-order PLL.

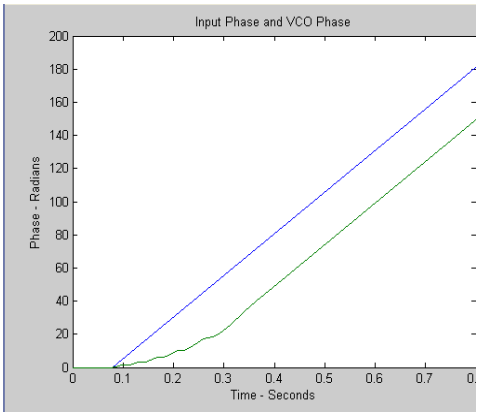

Fig 3.1 the input phase and the VCO phase

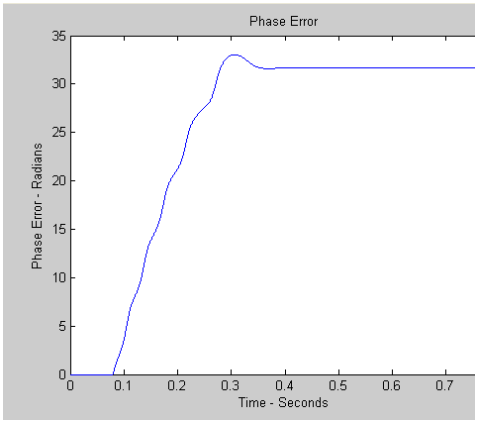

Fig 3.2 Phase error

In Fig 3.1 the blue line represents the input phase, the green line represents the VCO phase, it is shown in Fig3.1. The phase change of the input signal is linear with time, The slope of VCO phase equals to the slope of the input signal phase after experiencing a period of the curve, and the output phase achieves stability follows the input phase. We can see that after the PLL starting to work, in the first period of time, Input Signal After going through the phase detector and the loop filter, the input signal will be fed back the output phase to the VCO, which will let the VCO frequency gradually achieve synchronization with the input frequency, maintain a constant, and achieve lock finally. Where the PLL experiences the state of out of lock, tracking, capturing, and locked, and then finally reaches a steady state.

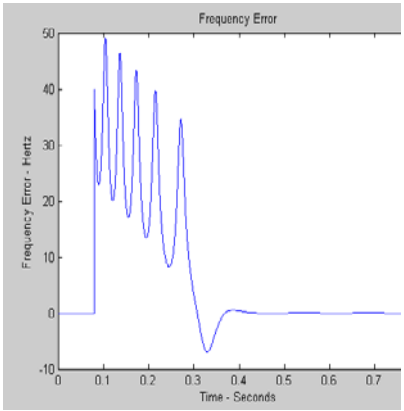

Fig 3.3 the frequency difference

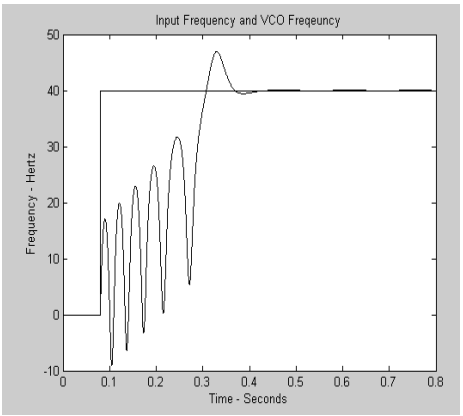

Fig3.4 the Input Frequency and the VCO frequency

Fig 3.3 and Fig 4.4 shows the process that the PLL goes through from out of lock, tracking, capturing, and locked after the PLL has worked. The process that the frequency changes from swinging to straight line state is called locking process. In the capturing process we can find that, with the increase in the number of capturing, the capturing process becomes slower, this shows that the frequency of PLL is working at the dynamic boundaries of stable operation at this time, and is working properly

Summary

This paper has finished the simulation of second-order PLL, and analyzed its simulation results. The experimental results showed that: the second-order phase-locked loop simulated using MATLAB achieves as originally envisaged, the state of out of lock, tracking, capturing, locked are all reflected, and the Simulation reaches the initial requirements.

References

[1] L.N. Arruda,S. M.Silva,and B.J.C.Filho. PLL structures for utility connected systems. 36th Annu. Meeting IEEE Ind. Appl. Conf. Rec. 2001

[2] K. G. Masoud,M. R. Iravani. method for synchronization of power electronic converters in polluted .and variable-frequency environments. IEEE Transactions on Power Systems. 2004

[3] Banislav Djokie,Eddy So. Phase measurement of distorted periodic signals based on nonsynchmnous digital filtering. IEEE Trans.on Instrum.Meas. 2001

[4] Shayan Y R,Le-Ngoc T.All digital Phase-locked loop: concapts,design and applications. IEE Proceedings. 1989

[5] Stephen M Walters,Terry Troudet.Digital phase-locked loop with jitter bounded. IEEE Transactions on Circuits and Systems. 1989