The introduction of disturbance observer in power system

Wang Xi[1, a], Ding Lijie[1, b], Zhang Hua[1,c]

[1]Sichuan Electrical Engineering Research Institute of State Grid, Chengdu 610000, China

[a]email:wangxi_55@sina.cn, [b]ding_lijie@163.com, [c]zhanghua002@163.com

Keywords: power system; disturbance observer; dynamic performance

Abstract. Most controllers used in power system such as PID controllers are based on linearization without considering the external disturbance. In this paper, the disturbance observer is introduced in HVDC control. Firstly, the model of HVDC system considering the disturbance is established. Then disturbance observer is designed to improve the dynamic performance of HVDC control system. Finally, a simple test system is used as an example to verify the validation of the proposed strategy. Simulation results show the superiority of the proposed disturbance observer compared with conventional controller.

Introduction

HVDC (High Voltage Direct Current) transmission technique is playing a more and more important role in large interconnected power system. On one hand, HVDC system has economic and technique advantages in transmitting large scale power to remote areas. On the other hand, proper control of HVDC is an effective way to improve the transient stability of interconnected system, due to its fast response and good controllability in control the DC transmitted power. [1-6]

Several researches have focused on the use of HVDC controller to improve the transient stability of power system in the past years. Most of the designed controllers such as PID controllers are based on the linearization of the power system around the steady state operation point. While the system is actually highly nonlinear, the change of operation condition or unexpected disturbance may lead to big variance of operating point. In this way the effect of linear controller may be weakened.

To have a satisfactory control performance, the exact knowledge of disturbance is needed, which is not easy to obtain in real system. To solve the problem, the DO(disturbance observer) is introduced in HVDC control in this paper. Firstly the system model of HVDC system is established, then the disturbance observer for HVDC system is designed to enhance the transient stability of the system. Finally the validation of the designed disturbance observer is verified in a 4-machine system.

System Model

HVDC system is usually simplified as a first order inertia model. The external disturbance such as high frequency noise, measurement error are also considered in the HVDC modeling.

$$\dot{P}_{dc} = (-P_{dc} + P_{dc0} + u_{dc}) / T_{dc} + d(t) \tag{1}$$

Where P_{dc0} is the reference value of HVDC power, u_{dc} is the control output of HVDC, T_{dc} is the time constant of HVDC model, $d(t)$ is the bounded external disturbance. $|d(t)| \le D$.

Disturbance observer

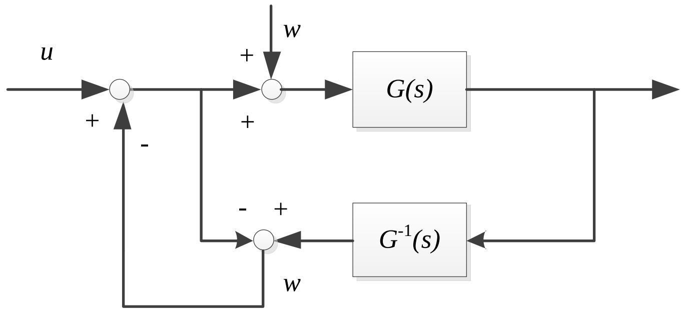

Fig.1 Block diagram of disturbance observer

Consider the following system

$$\begin{cases} \dot{x}_1 = x_2 \\ \dot{x}_2 = f(x) + bu + w \end{cases} \tag{2}$$

Where w is the disturbance and $|w| \le W$.

The basic principle of disturbance observer is to observe and compensate the system external perturbation, and then the system can be transformed into a non-interference model. For system (2), the DO can be designed as

$$\dot{\hat{w}} = L(\dot{x}_2 - f - \widehat{b}u - \hat{w}) \tag{3}$$

Where $\hat{w}$ is the observed disturbance, Substitute (2) into (3), we yields

$$\dot{\tilde{w}} + L\tilde{w} = \dot{w} \tag{4}$$

Where $\tilde{w}$ is the observation error and $\tilde{w} = w - \hat{w}$, $\dot{w}$ is the derivative of actual disturbance. The actual disturbance is assumed to be slowly varying compared with the DO dynamics. Thus, $\dot{w} = 0$. According to (4), the observation error can converge to zero exponentially with a positive L. Translate the output of DO into the control variables.

$$u_{do} = \hat{w} / \hat{b} \tag{5}$$

The control output of DO is overlaid onto the output of original controller, then the original system can be transformed into an approximate non-interference shown as (6).

$$\begin{cases} \dot{x}_1 = x_2 \\ \dot{x}_2 = f(x) + b(u - u_{do}) + w \approx f(x) + bu \end{cases} \tag{6}$$

Since the system disturbance has been greatly reduced or even eliminated, the control quality can be effectively improved.

Design of Disturbance observer in HVDC system

The design of disturbance observer in HVDC system in this paper is mainly used to enhance the transient stability of AC/DC interconnected system, the disturbance observer is designed as

$$\dot{\hat{d}} = L(\dot{P}_{dc} - \frac{-P_{dc} + P_{dc0}}{T_{dc}} - \frac{u_{dc}}{T_{dc}} - \hat{d}) \tag{7}$$

Translate the disturbance observer output into control variable

$$u_{do} = T_{dc}\hat{d} \tag{8}$$

Simulation Examples

To verify the validation of the propose HVDC supplementary controller, a 4-machine system built in electromagnetic transient simulation software PSCAD/EMTDC is taken as example. The single line diagram of test system is shown as Fig.2. In the system, the modeling of generators includes excitation regulators and speed governors, and the HVDC transmission system is simulated with a detailed HVDC control model.

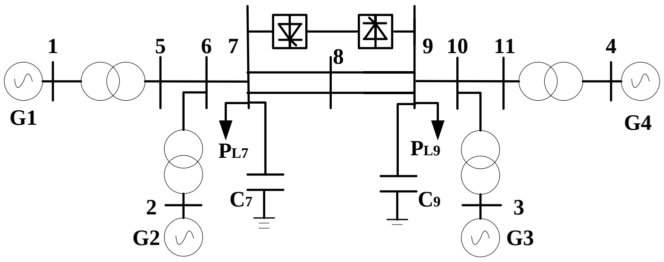

Fig.2. Single line diagram of the test system

The system with disturbance observer should have advantages in control performance when the system suffering from disturbance. To verify this, the following scenarios are considered in the simulation.

A sinusoidal perturbation with 0.01pu amplitude is added to the HVDC current reference signal at 4s. The time domain simulation of HVDC transmission power is shown as Fig.3, in which the control performance with and without DO (disturbance observer) are both presented.

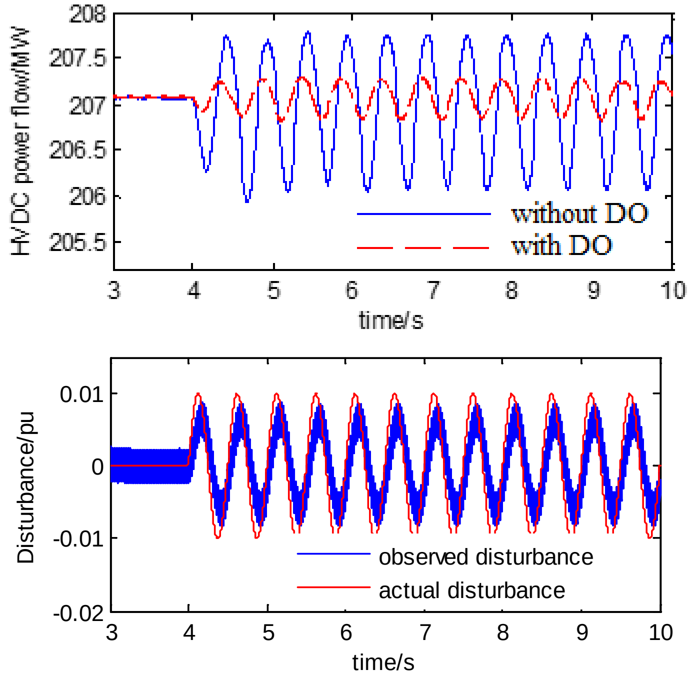

Fig.3.Time domain response under persistent disturbance (b)HVDC power flow.(c)actual disturbance and observed disturbance

It can be seen from Fig.3a that the oscillating amplitude of system variables is smaller when the disturbance observer is utilized. The main reason is that DO effectively observes and compensates and external disturbance, then the system with DO is less affected by the sinusoidal perturbation. Fig.3b shows the imposed disturbance and the disturbance observed by DO. We can see that before the sinusoidal perturbation is added, the main disturbance observed by DO is the system high-frequency noise. After the sinusoidal perturbation is added, DO rapidly tracked the perturbation and compensate to the system, so that the system with DO has better performance in anti-interference.

Conclusions

In this paper, the disturbance observer is introduced in HVDC control. Firstly, the consideration of HVDC external disturbance makes the controller more adaptive to the actual operation condition. Then disturbance observer is an effective way in dealing with unknown disturbance. Finally, a simple test system is used as example to verify the validation of the proposed strategy. Simulation results show the superiority of the proposed disturbance observer compared with conventional controller.

Reference

[1] IEEE Power Engineering Society System Oscillations Work Group, Interarea oscillations in Power system, IEEE 95-TP-101, Oct, 1994.

[2] M. E. Aboul-Ela, A. A. Sallam, J. D. McCalley, A. A. Fouad, Damping controller design for power system oscillations using global signals, IEEE Trans. Power Syst. 11(2) (1996) 767-773.

[3] Zhang Yang, Anjan Bose, Design of wide-area damping controllers for interarea oscillations, IEEE Trans. Power Syst. 23(3) (2008) 1136-1143.

[4] T. Smed, G. Andersson, Utilising HVDC to damp power oscilla-tions, IEEE Trans. Power Del. 8(1993) 620–627.

[5] Wang Juanjuan, Fu Chuang, Zhang Yao, Design of WAMS-Based Multiple HVDC Damping Control System, IEEE Trans. Smart Grid. 2 (2) (2011) 363-374.

[6] CIGRÉ Task Force 38.02.16, Impact of the interaction among power system controls, Paris, Technical Report. Fall 1999.