A Circuit Fast Fault Diagnosis System Developed with PODEM Algorithm *

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Abstract—**this paper deeply studies the fault models of digital circuits and proposes a combined implementation of BIST test mode, on the basis of which a new implementation of PODEM is proposed. In addition, this paper also studies the generation of test vector algorithm and a fault diagnosis system for special purpose equipment is designed and implemented based on the research in this paper, which wins the 2nd prize in a province level.**

Keywords—PODEM, fast fault diagnosis, BIST, SCOAP, dirigibility, observability.

I. INTRODUCTION

With the development of technology, especially for the digital electronic, the complexity of integrated circuit has increased. And this trend inevitably adds the difficulty for testing, thus increasing the designing funds and time consuming. In the circuit design nowadays, test has become a vital part.

Fault detection and location is the core of test, the digital circuit consists of Gate-Level, Chip-Level, Board-Level and System-Level. But, the test cost is in exponential relation with the size of chip, when the MHz increases, the cost will increase in exponential ways. To solve this problem, scientists raised many solutions. Early in 1966s, Roth et al proposed D algorithm [1] for the first time, which adopts the ideal of multidimensional sentisization, but it also has many problems; in 1981 Goel proposed PODEM algorithm based on D algorithm and made improvement [2]; Rozkovec M et al [3]proposed a function-oriented circle test method, which can fulfill the test without increasing the cost, but it has the problem of low cover rate for circuit fault towards those circuit based on FPGA; Nazar G [4] et al proposed a double-model redundancy method, which can achieve online test with comparison between two outputs, but it has rather high extra cost; document [5] proposed a multipath search parallel test vector generation algorithm (NBMP); algorithm [6] is an official mature and effective structure test algorithm aimed for combined-gate circuit. And Chinese experts also made many contributions to this field, Yinhe Han proposed a circuit test compression method [7] and uses some self-assemble big circuit to testify the

method; Yudan Deng developes a digital circuit generation platform based on Windows.

This paper mainly studies the automatic test vector generation algorithm for digital circuit, to achieve the fault character extraction, pre-processing, multi-resource fault sign integration, fault fast reasoning and other demand design, then propose a PODEM implementation, finally achieve the design and implementation of a diagnosis system for a special purpose equipment.

II. BUILT-IN SELFTEST

Built-In SelfTest(BIST) means system conducts configuration and test to itself through certain methods, which has a short cycle, easy implement and high fault cover rate and other advantages. With the complexity of circuit increasing, BIST is gaining more focus.

When the chip and system is conducting BIST, generally it needs test figure generation circuit, test circuit, data compressing circuit, as shown in Fig.1. Test figure generation circuit generates the test figure, and load it to the test circuit through timer, data compressing circuit mainly conduct the compressing response signal to reduce the room cost, and comparison circuit compares the input signal and
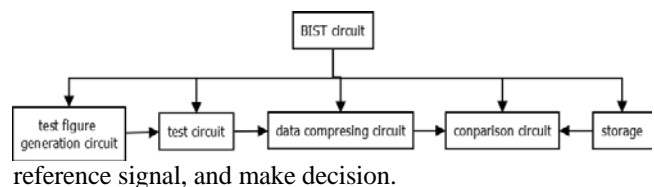

reference signal, and make decision.

Fig. 1. structure of BIST

According to the demand of system, here we main introduces the method combines deterministic test and random test.

III. THE GENERATION OF TEST EXCITATION VECTOR

After the PCBA modeling of PCB, stimulation should be posed to circuit model based on the given excitation. Circuit stimulation is divided into two parts of good board and fault. The good board stimulation is to conduct

stimulation on no-fault circuit. Through this stimulation, we can obtain response and analyze time condition of normal circuit. The fault stimulation is to set various faults to the circuit to analog the situations may occur in the normal usage, and conduct stimulation to it then obtain the response. Through the comparison of good board and fault stimulation, if the result doesn't match, then it's considered that the fault is detected.

A. Measurement on testability

The concepts of dirigibility and observability of circuit signal origins from Automatic Control Theory. The dirigibility of digit circuit is defined to the degree of difficulty of setting certain logic signal to 0 or 1, and the observability of it is defined to the degree of difficulty of observing the state of logic signal. These measurements are vital to the generation circuit test excitation vector, because there are several methods to observing the inner signal, but cost should be taken into consideration, through loading signal on primary input and sending the value of inner signal to primary output, the cost can be remarkably reduced. The measurement of dirigibility and observability can be proximately quantified to the difficulty of setting and observing the inner signal of circuit. And the analysis of testability has two features:

- It's the analysis on circuit top logic, but not a test vector, it belongs to static analysis;

- It owns a linear complexity, or it's of no sense, because it can be generated with automatic test vector or stimulated with fault.

The SCOAP measurement on testability, raised by Goldstein in 1980, is a systematical and effective algorithm to calculate dirigibility and observability, which is still widely used now. SCOAP prescribes that every node in circuit can be described with 6 parameters:

- Unit 0 dirigibility $CC0(n)$

- time order 0 dirigibility $SC0(n)$

- Unit 1 dirigibility $CC1(n)$

- time order 1 dirigibility $SC1(n)$

- Unit obervability $CO(n)$

- time order observability $SO(n)$

Generally, 3 unit measurement is related with the quantity of signal which can be used to control or observe n, 3 time order measurement is related with the quantity of time frames (or time circle) which needs control or observation. Dirigibility ranges from 1 to infinity, while observability ranges from 0 to infinity. The larger the value is, the more difficult the control and observation will be.

Definition 1: to set node n to unit logic value 0(1), the least times of assignment needed to set related node to decide unit logic value is called the Unit 0(1) dirigibility value of node n, represented with $CC0(n)(CC1(n))$.

Definition 2: to set node n to time order 0(1), the the least times of assignment needed to set related node to decide time order logic value is called the Unit 0(1) dirigibility of node n, represented with $SC0(n)(SC1(n))$.

Definition 3: to send the information of node n to primary output, the least times of assignment to unit logic value needed is called unit observability value of node n, represented with $CO(n)$.

Definition 4: to send the information of node n to primary output, the least times of assignment to time order logic value needed is called time order observability of node n, represented with $SO(n)$.

Circuit series should be taken as reference value when calculating dirigibility and observability. The series of circuit nodes between input and output is the path from PI(Primary Input) to PO(Primary Output), taking the longest path from PI as the series of circuit nodes. The series marking algorithm from PI to PO is described as follow:

1) Assign all PI with series 0;

2) Fan out every with:

a) With PI series marking circuit connection

b) Adding fan-out drive logic module to queue

3) When the queue is not empty:

a) Extract a logic module from the queue

If the logic module has already marked all the fan-in, then use the max value of input series plus one to mark the logic door and its fan-out, and add the logic module fan-out by drive logic module to queue. Otherwise, add this logic module into queue again.

The node series from PO to PI is along the path from PO to PI, the shortest path from PO is the series of circuit nodes. Method of marking series from PO to PI is similar to above, the only difference lies on the marking start point, PO.
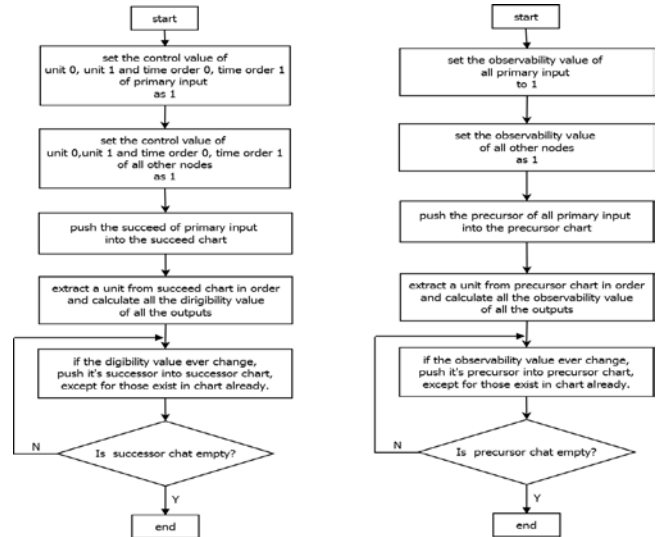

Fig. 2. flow chart of dirigibility value calculation

Fig.2 is the flow chart of SCOAP algorithm calculating random node n's dirigibility value $CC0(n)$ and $CC1(n)$ and observability value $CO(n)$. First a queue chart(first in first out order, FIFO in short) should be built, called successor chart. Successor means that starting from the circuit input, calculating the dirigibility value of circuit nodes level by level to the primary output. Every calculation should take a unit from successor chart in order, then access the dirigibility database of standard unit to calculate the value.

To make it easier, SCOAP builds a FIFO queue chart called precursor chart. Precursor means that starting from the circuit output, calculating the observability value in the reverse order. This calculation also take a unit from chart in

order, then take observability database of standard unit and dirigibility obtained already to get the observability value of all input. For those fan-out nodes, take the minimum observation value in all the fan-out branch as the value of fan-out root node.

B. Deterministic test generation algorithm PODEM

The generation of test excitation vector is procession of automatically generating the test excitation vector for circuit to be tested through computer or other tools according to certain generation algorithm. Goel proposed that the runtime of generation algorithm and the square of number of circuit gate is directly proportional, when the circuit size grown with n, the runtime grows with n2. In the aspect of algorithm complexity, the generation problem is about nonlinear polynomial complexity, that is to say, there is no algorithm can solve this problem in linear time limitation. Thus, it remains a problem to obtain effective test excitation vector in a rather short time.

The idea of PODEM algorithm is: trace the activated fault backward to primary input, search all possible primary input assignment, to get a qualified one to serve as test excitation vector, algorithm end. This algorithm is based on circuit structure test, taking the circuit net as research object, reduce number of the return operation, it works well in most cases, accomplishing a satisfying fault cover rate.

The algorithm has randomness when assigning the primary input, it adopts the branch-decision tree to solve the assignment searching problem. For every primary input port(PI), there are two possible input, thus they can be probed in one time, resulting in binary tree in Fig.3.
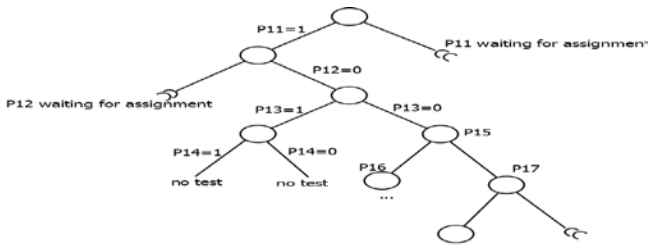

Fig. 3. branch-decision tree

Non-test show two possible situation: the first is the value of decided PI's fault point equals the fault value, failing to activate the fault; the second is decided PI already has cut the connection between the fault scene and PO, the fault connection is not sensitized.- In these two occasions, PO cannot observe the fault signal, thus according test vector is not test excitation vector. The algorithm flow chart of PODEM is shown in Fig.4.
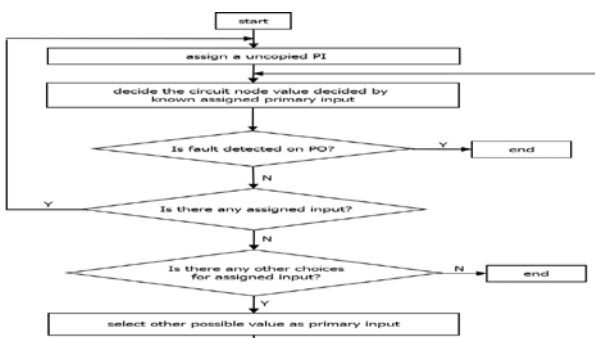

Fig. 4. flow chart of PODEM algorithm

In PODEM, the logic analysis and calculation on fault circuit and non-fault circuit corresponds to the D-drive in D algorithm, but the reverse implication is included in the procession of deciding the primary target and PI. The differences between two algorithm is: D-drive in D algorithm is random in direction, while the PODEM must figure out the shortest path between fault signal D and PO to conduct the drive; when conducting reverse implication, PODEM chooses the most easy and the most difficult path, which is obvious in target, also has a high success rate, reducing the times of return and improving the running speed.

IV. THE DESIGN AND IMPLEMENTATION OF A FAULT DIAGNOSIS SYSTEM FOR SPECIAL DESIGNED EQUIPMENT

Based on the technology above, we design and implement a special designed equipment fault diagnosis system, which is aimed for a special designed equipment and can conduct fast fault diagnosis for Mainboard module and I/O interface module, it also can give reasonable advice for the fault. This system has the high efficiency, low cost and it's easy for extension.

A. General structure design

The fault detection system consists of 6 parts: interface part, mainboard diagnosis part, I/O interfaced diagnosis part, master control part, fault information output part and fault diagnosis software part. Structure of system is shown in Fig.5.
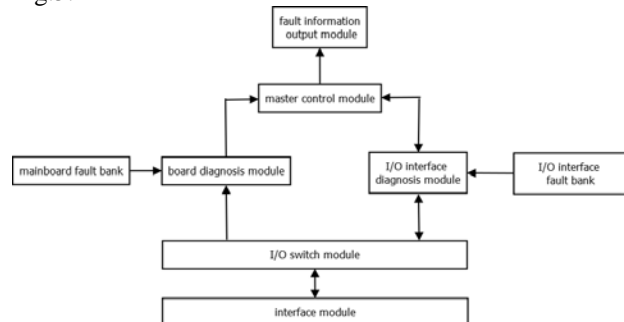

Fig. 5. structure of diagnosis system

Here we mainly introduce two core modules which take advantage of technology mentioned above and give a brief summary of other modules.

B. System board diagnosis modules

This module is designed based on BIOS Post self-diagnosis function of system board, which is in charge of the diagnosis of main board and relative boards.

C. I/O Diagnosis Module

This module is in charge of I/O interface module and related board fault diagnosis. On the one hand, I/O interface diagnosis module is connected to the equipment through ISA& PCI& AGP, on the other hand, I/O interface module is connected to printer through serial and parallel port. When diagnosis is being conducted, I/O interface diagnosis module firstly conducts loop back test on communication chip and obtain result through the serial port. According to the result, the module will give relevant advices to the LCD panel and display the fault status through status light. The structure of this module is seen in Fig.6.
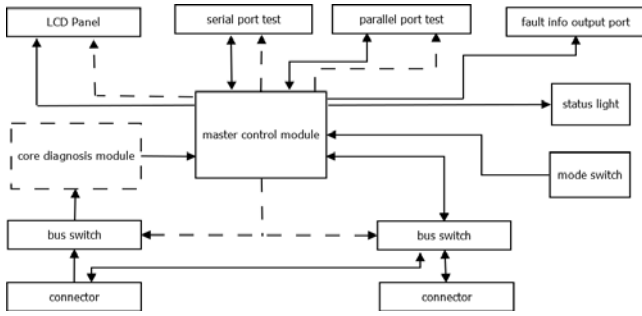
Fig. 6.   Structure of I/O diagnosis module

D. Master control module

This module is in charge of the running of diagnosis software and the management, control of relative soft/hard ware sources, the structure of which is shown in Fig. 7. To guarantee the speed of system, the CPU of S3C2410 based on ARM920T core is adopted in this module, which has an external frequency of 12 MHz, hitting 230 MHz after internal frequency doubling. The master control module achieves LED control/display interface, states light control interface, main board faults code collection interface, I/O interface control/data interface, system serial control/data interface and system LPT control/data interface through GPIO pin and internal controller, which provides functions like LED display, collection of fault codes, serial communication, etc.
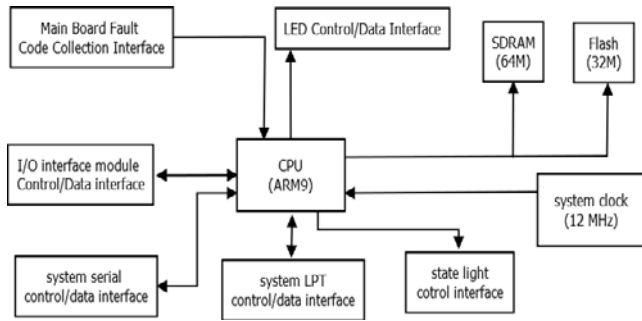

Fig. 7.   structure of mater control module

E. Diagnosis software module

The flow chart of diagnosis is shown in Fig.8. The diagnosis card runs after the POR. the software firstly decide the diagnosis mode.
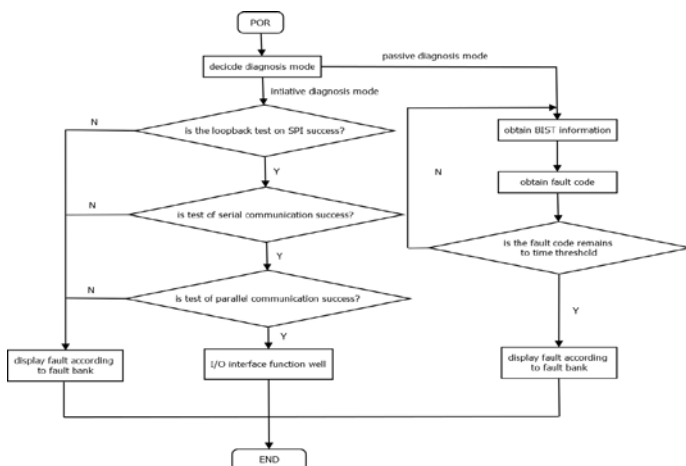

Fig. 8.   Flow chart of diagnosis software

if it is in the initiative diagnosis mode, it firstly initiates the communication part in I/O module, and conducts loopback test to the SPI, if it succeeds, then starts the serial communication test, if it passes, then starts the parallel communication test. If the system fails in any step of the test, it will give out the fault information in reference with the fault bank, otherwise the equipment works well.

In the passive diagnosis mode, the software firstly obtain the BIST information and latch. System will calculate the living time of the fault code, if it exceeds the threshold, system will give the fault information in reference with the fault bank, otherwise it will recalculate the exist time and repeat the steps above.

F. Diagnosis output module

This module could output the diagnosis result to desktop work station through dedicated port in a fixed formation, which could achieve seamless connection between remote maintenance system and diagnosis system.

V. CONCLUSION

This paper deeply discusses the research condition of digital circuit test home and aboard. Then we discuss the BIST, PODEM and SCOAP algorithm, based on which we propose a test vector generation algorithm which combines the deterministic and random test. Adopting that algorithm as the BIST vector generation module, we design and implement a core part of a diagnosis system for a special designed equipment.

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