Research on an Improved Power Factor Correction Method Based on Single-Cycle Control

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Abstract. Analysis the conventional topology of Boost power factor corrector and input equivalent circuit and point out that conventional topology of Boost power factor corrector exists with improvement of converter power and the switching frequency. The efficiency of system is greatly reduced. The paper proposes a modified Power factor corrector ,analyzes the modified Boost circuit topology ,basic principle, analyzes the improved one-cycle control equation of the circuit, give the selection of parameters of the main components with theoretical basis，analyze the design of control system of the PI regulator in theory and calibrate the control system as typical Ⅱ type system, improve the anti-jamming ability and stability of the system, and make a prototype to prove the validity of theoretical results.

Introduction

With the development of power electronics technology, more and more power into the grid rectifiers used in the benefit of the power industry, but also to the large number of harmonics injected into the power grid, APFC (Active Power Factor Correction) active power factor correction also It has become a hot research scholars, traditional Boost power factor correction circuit because the circuit by MOS transistor switching frequency f_m limit [1-5], based on the OCC (One Cycle Control) power factor can reduce the multiplier and input voltage detection circuit, many scholars single and three-phase conversion are made based on one week of PFC circuit, based on the principle of quasi-steady state control, OCC PFC converter can be considered as deemed to DC-DC conversion architecture steady-state operation of the switch in a single week, if the input from end control phase voltage and phase current ratio is a constant, it can be regarded as a power factor of 1.

At present, most research focuses on the power frequency f_1 (50Hz) case, as shown in Figure 1 is a schematic diagram of a conventional single-cycle controlled Boost converter, namely: after bridge rectifier connected Boost circuit, a power correction circuit can be removed later in the bridge rectifier the large filter capacitor C, so that the output voltage of the rectifier behind half sine wave, Boost will change just by changing the duty cycle of the sinusoidal output voltage is higher than the maximum constant DC voltage, which is to monitor the core essence of the half-wave rectified half-wave voltage, the current tracking voltage, Boost converter will rise and fall along the half-sine curve different voltage into a DC voltage principle is, in a period T switch S1 is turned on for some time T_{ON}, energy storage inductor L, when the switch S1 is turned off, the inductor L are reversed polarity.

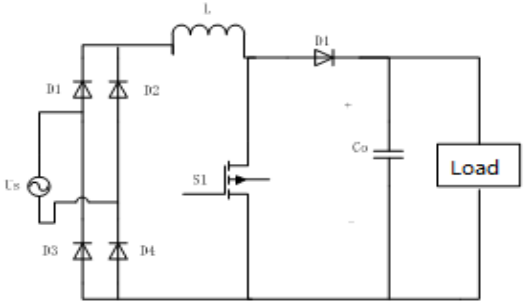


Fig 1 Schematic of conventional boost converter

When the dot L end of the inductor voltage rises higher than the input voltage V_{in}, switch off S_1, during storage of T_{ON}, the inductance energy to provide energy L to the load through VD, this converter output - input voltage relationship as follows:

$$V_O = \frac{V_{IN}}{1 - T_{ON}/T} \qquad (1)$$

The main task of the power factor correction circuit is the use of Boost converter will be converted into stable along half sine wave voltage rise and fall of nowhere than the maximum amplitude of the input sinusoidal voltage slightly higher DC voltage output, power factor correction circuit of the second circuit the main task is to detect the input current of the power grid, and input it into the grid voltage sinusoidal phase [7-8]. The main principle is to control the chip grid sampling of current and sinusoidal current reference is compared, the difference between these two sine waves will produce an error voltage, the error voltage to adjust the turn-on voltage, so that the grid current sample and the reference sine currents have the same amplitude and phase, in Figure 1, the sine positive throughout the period, there will always be two four bridge rectifier switching devices will be turned on, regardless of the stage portion sine positive or negative axle axle there will be a freewheeling diode or a MOS transistor is turned on at all times, so that any three of the switching device is turned on, the increase with the increase of the switching device and switching frequency, switching losses P_S will increase, the overall system loss P_z will increase, so that the overall efficiency will be reduced. To solve this problem this paper from OCC PFC circuit structure analysis, to provide an improved OCC PFC circuit, it is possible to improve the stability and robustness of the system.

General OCC PFC Converter Input Equivalent Circuit and Analysis

This paper analyzes the single-phase OCC PFC circuit, Figure 2 shows the main single-phase OCC PFC main circuit topology, within a period of the output voltage U_o can be considered constant amount, the entire controller output steady-state value, wherein U_m is the input sampling resistor grid, the transfer function $H_{V(S)}$ is the voltage control.

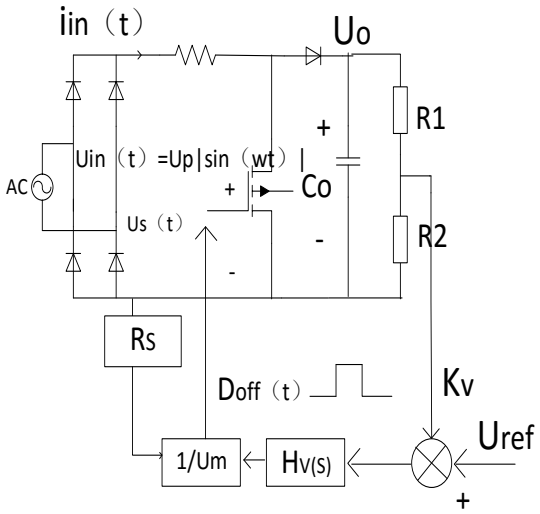


Fig 2 OCC PFC converter chart

Throughout the several consecutive switching cycles AC / DC converter can be considered as steady-state operation of DC / DC converter circuit, so the input voltage $U_{in(t)}$ and the reference voltage U_{ref} circuit, which can be approximated by the equation.

$$U_{in(t)} = D_{off} U_{ref} \qquad (1)$$

Wherein D_{off} is the switch off when the duty cycle, but also by the input D_{off} current sampling resistor $i_{in(t)}$ and the product of the entire controller R_S steady-state output ratio based on the calculated parameters, the parameters U_m are calculated as follows:

$$D_{off} = \frac{i_{in}(t)R_S}{U_m} \qquad (2)$$

We need to get the equivalent circuit of FIG. 3, the circuit by the presence of the following equation,

$$U_{in(t)} = i_{in(t)}R_{eq} \qquad (3)$$

Among them, the equivalent resistance is as follow.

$$R_{eq} = (R_S U_O)/U_m \qquad (4)$$

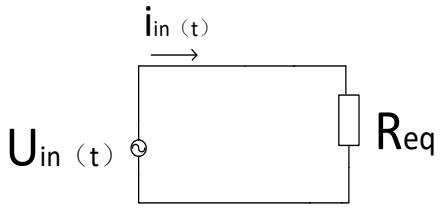


Fig 3 OCC PFC input equivalent circuit

Improved PFC Circuit Diagram

According to the literature [5], improved PFC circuit, as shown, the circuit analysis theory,

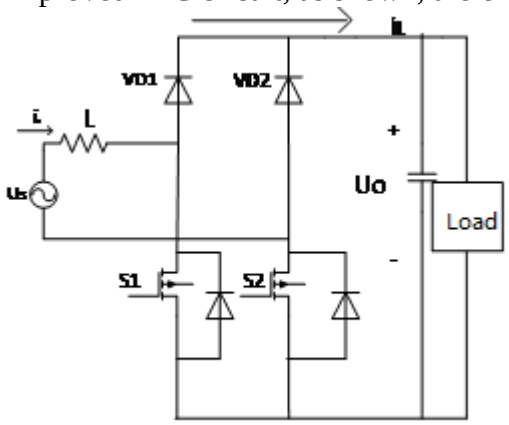


Fig 4 Improved PFC circuit topology

Circuit can be broken over the entire period of four states circuit schematic [9-12], the four kinds of equivalent circuit diagram, the positive half cycle of the sinusoidal AC circuit, the equivalent circuit diagram of two 5

For the Fig. 5 (a) circuit, the positive half cycle sinusoidal voltage alternating current for charging the inductor L, closing switch MOS transistor S1, VD_4 controlled conduction, this state capacitor C_O to provide energy load; when closed MOS transistor S1, which is equivalent to circuit shown in Figure (b) inverting the polarity of inductor L, S2 controlled anti-parallel parasitic diode conducting, for powering loads while capacitor C_O is charged.

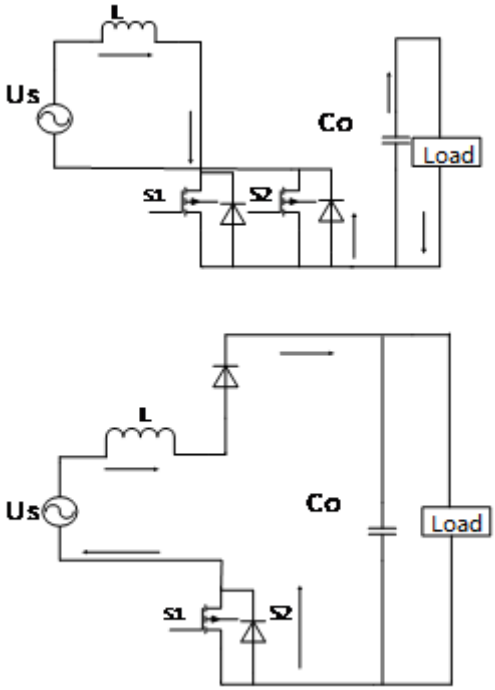


Fig 5 The half circle sinusoidal voltage

Sinusoidal voltage negative half-cycle time, work time equivalent circuit diagram of the circuit shown in Figure 6, which works as follows, FIG. 6 (c) schematics, S2 is closed at this time MOS transistor is turned on, the flow through the switch S1 anti-parallel diode, and the capacitor load C_o, when the switch S2 is turned off when the inductance L of the polarity is inverted, VD2 conduction controlled to provide energy load while the output capacitor C_O to provide energy, S1 controlled anti-parallel diode is turned on.

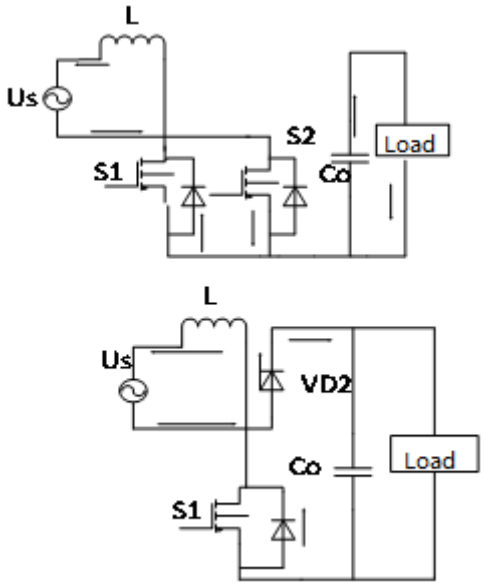
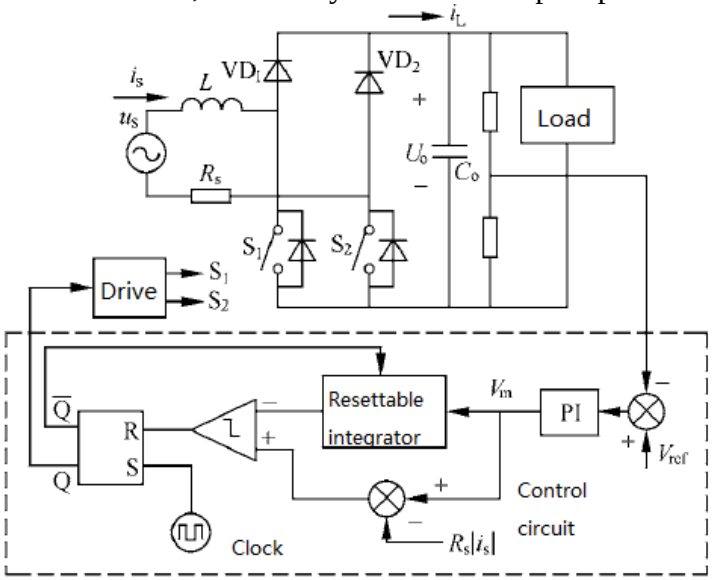


Fig 6 sinusoidal voltage negative half-cycle

Based on the above analysis, the conventional single-cycle control of power factor correction, there are three switching device is turned on, the improved power factor correction has two switching devices turned on during any period in any period since the MOS S1 and S2 common ground, so no external isolation circuit, driving circuit is simple, due to lower power consumption, it is suitable for medium and high-power applications.

The Main Control Schematic of Improved Power Factor Correction Circuit

One cycle control controls core idea is to make the average of the control object and switch variables in each period of the reference amount is proportional to [13]. Since the switch tube drive circuit is simple and a frequency fixed amount, the circuit design PWM drive output selecting circuit has two opposite PWM circuit, commonly used are: D flip-flop.



Next, the circuit diagram parameters detailed derivation and calculation, as viewed from the AC input, assuming power factor correction is 1, the Boost converter is purely resistive, can be equivalent to R_{eq}, and get control of the objective function needs.

$$R_{eq} = \frac{u_s}{i_s} \qquad (5)$$

Wherein: u_s is the input AC voltage.

i_s is the current value of the AC input.

Since the positive and negative half cycles which are equivalent to the same Boost converter circuit, so the relationship between the input and output stabilizing circuit output voltage can be equivalent to,

$$U_o = \frac{|u_s|}{1 - D_{on}} \qquad (6)$$

Wherein: U_O is the terminal voltage across the load.

D_{on} is Duty MOS tube at work.

Consolidation (5) and (6) in accordance with the principle of equal afford,

$$R_{eq} i_s = U_o (1 - D_{on}) \qquad (7)$$

To obtain the resistance of the sample with the sampling voltage U_s, the equation (7) is multiplied to both sides of the sampling resistor R_s, to give

$$R_s R_{eq} i_s = U_s R_{eq} = U_O (1 - D_{on}) R_s$$

$$\text{Set } U_P = \frac{R_s}{R_e} U_o \qquad (8)$$

One cycle control is obtained control equation

$$(1 - D) U_p = R_s i_s \qquad (9)$$

To (8) on both sides simultaneously integrating in a switching cycle,

$$U_p - U_s = \frac{1}{T_r} \int_0^{T_r} D_{on} V_m dt \qquad (10)$$

(9) equation can be used to build the circuit, with resistance division method to collect the load

terminal voltage, and set a good reference voltage U_{ref} op amp for the poor to obtain a difference U_e, a difference through PI regulator output U_m, will be U_m and U_s

Subtraction op amp integrator amplifier configured as a comparator, the output value reached when the difference between when the comparator output inverted, the integrator is reset while the reset signal [14].

Design of Single-Cycle Control PI Regulator

Single-week performance PFC control circuit that controls the ultimate goal is to make the output of the voltage U_o stability, according to $U_P = \frac{R_s}{R_e}U_o$, the parameters U_o can be determined by U_p, according to the power of the input power is equal to the output power to give,

$$P_{out} = P_{in} = P_{load} + U_o I_{cin} = \frac{U_S^2}{R_{eq}} \qquad (11)$$

Wherein: P_{load} is the power consumption of the load

I_{cin}: Current flowing through the capacitor

According to $U_P = \frac{R_s}{R_{eq}}U_o$, get $R_{eq} = \frac{R_s}{U_p}U_o$. According to (11) to get

$$P_{load} + U_O I_{cin} = \frac{U_P U_S^2}{R_S U_O} \qquad (12)$$

Affect the actual design process of small signal perturbations

$$\begin{aligned} U_S &= \bar{U}_s + u_s \\ U_O &= \bar{U}_o + u_o \qquad (13) \\ U_P &= \bar{U}_P + u_p \end{aligned}$$

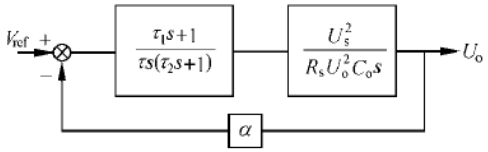
Wherein $I_C = \bar{I}_C + i_{cin}$, since the capacitance $\bar{I}_C$ is negligible, to get the number of transfer lines from i_{cin} to u_o.

$$\frac{u_o}{i_{cin}} = \frac{1}{C_O S} \qquad (14)$$

In order to obtain second-order system, adding inertia, provided the transfer function of the regulator

$$Q(s) = \frac{\tau_1 s + 1}{\tau s(\tau_2 s + 1)} \qquad (15)$$

It is located a block diagram of the control system are as follows



Period α is for the scale factor of the voltage detector, according to the optimal design type Ⅱ system, the bandwidth provided in the h = 5, the open-loop transfer function for the entire system,

$$q(s) = \frac{\alpha U_s^2(\tau_1 s + 1)}{\tau R_s U_o^2 C_o s^2(\tau_2 s + 1)} = \frac{K(\tau_1 s + 1)}{s^2(\tau_2 s + 1)}$$

$$\text{To get } \tau_1 = \frac{h+1}{2}\frac{1}{w_c}$$

$$K = \frac{w_c}{\tau_1} = \frac{\alpha U}{\pi R_s U_o^2 C_o}$$

The Verification of Experimental Data

The above analysis of the data, to design a PFC prototype 150UA improved one-cycle control, the DC output voltage = 50V, with DC electronic load under constant state current 3A, controlled MOS transistor switching frequency is 20KHz; inductors $L = 2mH$, DC side $C_o = 2200uF$; adjusting the output parameters

$$\tau_1 = 2.5ms, \tau_2 = 8ms, \tau_3 = 3.6ms, K = 3.3333$$

The experimental test using IV8711 Programmable DC Electronic Load Tester, programmed into the constant gear 3A, the entire system debugging circuit shown in Figure 9,

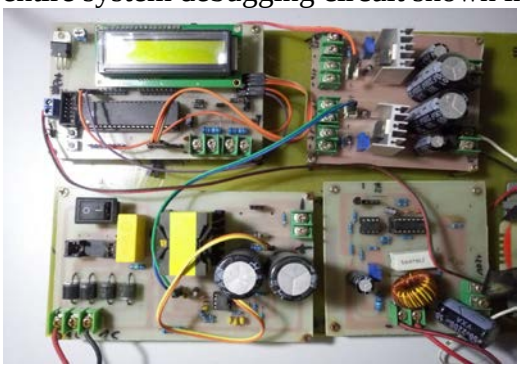


Fig .9 The production test system prototype

Uncorrected circuit current waveform distortion is very serious, you can use the THD (total harmonic distortion) to measure the size of the parameter value,

$$THD = \sqrt{\sum_{n=2}^{H} (\frac{G_n}{G_1})^2}$$

Calculated before uncorrected as 78.4%, single-cycle control PFC circuit that corrects the power factor drops to post, 150UA prototype measuring the input voltage and current waveforms in Figure 10, the current waveform serious distortion, power factor low

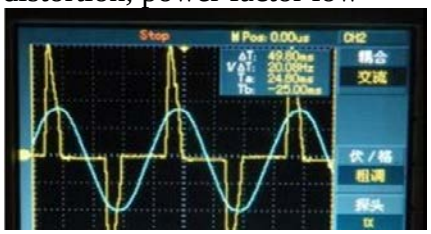


Fig 10 Improved power factor correction is not added to the system input waveform

After the addition of improved power factor correction system, the system follows the waveform shown in Figure 11,

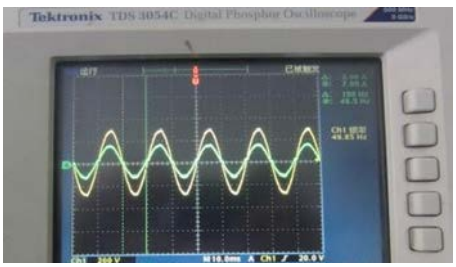


Fig 11 Improved power factor correction systems waveforms

The input current waveform tracking voltage, input power factor of 0.993-side measure, in order

to verify that the output circuit efficiency problems, this circuit measures the efficiency of multiple sets of data curve and power factor correction of the conventional single-cycle control output efficiency curves were compared, to see from the above data visualization to improve the efficiency of the system, the efficiency of the circuit diagram shown in Figure 12

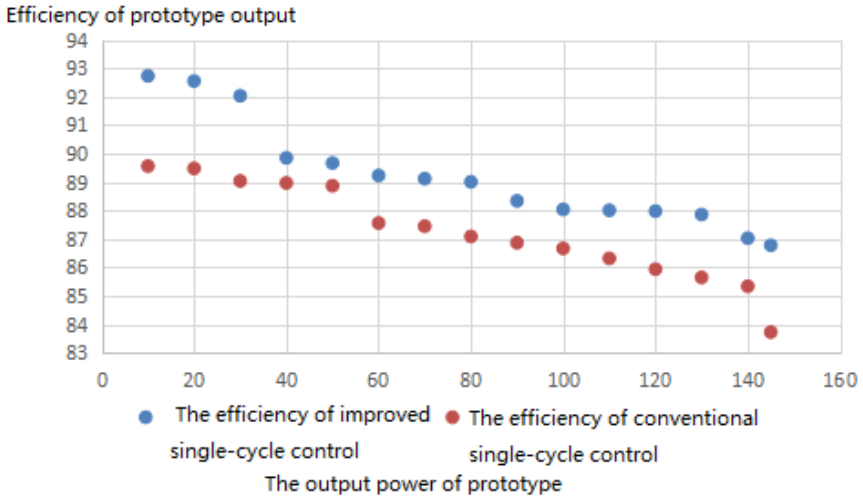


Fig 12 Improved contrast single-cycle control and the efficiency of a conventional single-cycle control

Conclusion

In this paper, based on one week of improved control of power factor correction circuit, first introduced the system circuit diagram of a conventional single-cycle control, and one-week power factor correction circuit principle of derivation, introduced conventional power factor correction circuit the main design steps, two main tasks, the first task is the output than the input sine half-wave peak voltage large stable DC output voltage, the second task is to track the input current sense input voltage [15]. Because it always has three switch circuit is turned on within the entire cycle, leading to its efficiency is not high enough, in order to solve this paper presents an improved power factor correction circuit analysis and derivation of single-cycle control equations of system design schematics, established a one-cycle control equation, and the most important design PI controller has been designed with the idea of derivation of its design, the final design with a 150W single week based on improved control of power factor correction the measuring circuit voltage and current waveforms with and without power factor correction circuit waveforms were compared, efficiency is improved by 2% -5%, the paper design is equally applicable to a single week FCATS device control.

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