3D-Partition: A Design Space Exploration Tool for Three-Dimensional Network-on-Chip

Ji Wu*
Computer Science and Educational Software, Guangzhou University, Guangzhou, China
*Corresponding author

***Abstract*—In this paper, we introduce a compositive model of fabrication cost, network throughput and power consumption, to explore different 3D design options of 3D NoCs. The model allows partition of IPs across different dies in 3D stack. Based on the model an estimation tool, 3D-Partition, is created and validated by comparing its results with those obtained from NIRGAM. Effects of various 3D NoC architectures under different 3D IC partition strategies on cost, throughput and power consumption are explored to demonstrate the utility of the tool. It provides economic and performance reference to designing 3D ICs for volume production in the future.**

Keywords-3D NoC; design space exploration; many-core processor design.

I. INTRODUCTION

The design of 3D NoC is a difficult process of searching for an optimal solution with functional (more and more complex applications) and non functional (power, area, cost, time-to-market) constraints. With the increasing number of design options, the design difficulties are aggravated. Conventional simulation based CAD tools are not time efficient enough to handle all these options at one time, hence design problems are de-coupled and explored sequentially, which lead to global sub-optimalities and a lot of iterations.

Recent research in this area has sought to address some of these issues. The example of such tool, Nessie, which is outlined in [1], can quickly explore many different system level options before deciding on the design space points he would like to explore in more details. But it's dedicated to SoC design, and can be extended to 3D environment, but not suitable for 3D NoC. Xie present a complete high-level simulation platform for 3D NoC called Meshim, but it's based on mesh topology without much variations[2]. There are other design space exploration tools, such as one for butterfly NoC[3], and another for designing application specific irregular 3D NoC topologies[4]. The objectives of these tools seek to improve some of the performance parameters including communication latency, area and power consumption under several 3D constraints. But none of them simulates all the parameters with all topologies. Nevertheless we don't know which topology we should choose at the early design stage and need to measure all of them. Furthermore, most of them focus on network performance, energy dissipation, and wiring area overhead, and neglect fabrication cost which would play an important part in whether an electronic product should be launched.

In this paper, we present a high-level exploration tool for 3D NoC (3D-Partition), which explores the architectural design space of 3D NoC at the early design stage. 3D-Partition uses a compositive model of fabrication cost, network throughput and power consumption, supporting six 3D NoC architectures, 3D mesh, hyper octagon, ciliated mesh, separate mesh, generic fat tree(SPIN) and butterfly fat tree(BFT), to explore different design options of 3D NoCs. It can evaluate more aspects and provide more options than existing 3D NoC exploration tools.

This rest of this paper is organized as follows. Section 2 illustrated the compositive cost model used by 3D-Partition, and proved the feasibility of it by comparing the simulation results with those from NIRGAM. In section 3, different 3D architectures under different partition strategies of a many-core processor are simulated using 3D-Partition, and thus utility of the tool is shown to help users to choose the best tradeoff among various design options. The implementation details are also presented in this section. The conclusion is presented in Section 4.

II. MODEL OF 3D-PARTITION

In order to explore the 3D NoC design space, we develop 3D-Partition, which searches for the optimized configuration that provides the best fabrication cost, network throughput and power consumption tradeoff according to the compositive cost model for a given number of different 3D partitions. The relative compositive cost for a given 3D NoC configuration is defined as

$$relative\_cost = \frac{fab\_cost}{fab\_cost_{baseline}} * W_c + \frac{throughput_{baseline}}{throughput} * W_t + \frac{power}{power_{baseline}} * W_p \quad (1)$$

where W_c, W_t and W_p are the weight of fabrication cost, throughput and power consumption respectively.

Actually the relative compositive cost model is the weighted average cost of relative fabrication cost, network throughput and power consumption. The weighted average is a traditional mathematics notion which is similar to an arithmetic mean (the most common type of average), where instead of each of the data points contributing equally to the final average, some data points contribute more than others. The notion of weighted mean plays a role in descriptive statistics and also occurs in a more general form in several other areas [5]. If all the weights are equal, then the weighted mean is the same as the arithmetic mean.

The weighted average cost is widely used, for example, Tsai introduced a weighted average cost to in design space exploration of 3D Cache [6], Meshkat proposed a Requirements based system level risk modeling [7]. These weight parameters can be set according practical requirements. The reason why we use relative cost instead of absolute data is that we want to eliminate latent errors brought by different underlying technology parameters, and relative cost, although not accurate, is enough for us to choose the best tradeoff among a large amount of design options, which is all that 3D-Partition need to do.

A. Fabrication Cost Model

Cost is the dominant factor for making decisions of whether a new technology should be adopted. Wu presents a fabrication cost estimation method for 3D ICs which include wafer cost and 3D bonding cost [8]. The cost model used in this paper is based on it

B. Performance Estimation

In order to clearly introduce 3D-Partition, some definition and correlative metrics should be stated first. We choose wormhole routing as the flow control methods where the network packets are broken into fixed length flits. The header flit holds information of the routing and control information. It establishes a path, and all subsequent flits follow that path.

Network throughput is a metric that quantifies the rate of successful message delivery over a communication channel. It is commonly defined as the average number of flits arriving per IP block per clock cycle, and in 3D-Partition, it's defined as the maximum throughput of a system which means the peak data rate that a system can sustain. In order to get the data, the simulation tool needs to firstly slowly increase the injection loads and run for 10000 cycles to allow the network to stabilize, and then for another 10000 cycles to get statistical data of throughput. The evaluation methodology comes from the established benchmarks of throughput and power consumption for NoC [9] and some complement for 3D NoC [10].

Power consumption, also called energy dissipation, is a vital character of network NoC structures. In NoC, it's measured by the energy consumed by the router and the inter-router wires. Similar to throughput, we also need to firstly increase the injection loads and wait for the statistics of a stabilized network, which means the maximum power consumption per cycle is what we want. The power consumed per flit per hop is given by

$$E_{hop} = E_{router} + E_{wire} \tag{2}$$

where Erouter is the power dissipated by each router, and Ewire is the energy consumed by inter-router wires. In order to acquire power characteristics, the routers of different 3D NoC architectures are modeled in VHDL. Then Synopsys Prime-Power is used to gather data of the energy dissipated by each router, Erouter , the results of which is shown in Table I. And we compute Ewire by estimate the capacitance, wire length and number of repeaters of wires.

Energy of a packet of n flits which traverse the network in k hops is given as

$$E_{packet} = n\sum_{i=1}^{k} E_{hop,i} \tag{3}$$

If N_{packet} packets are transmitted in t cycles, then the power consumption per cycle is given by

$$E = \frac{\sum_{j=1}^{N_{packet}} (n_j \sum_{i=1}^{k_j} E_{hop,i})}{t} \tag{4}$$

TABLE I. THE CONFIGURATION, STATIC POWER CONSUMPTION AND EMPIRICAL GATE COUNT OF ROUTERS

Router Type	Port Number	Router power consumption (pJ)	Empirical Gate Count (million)
3D mesh Router	7	94.1	1
Hyper octagon Router (+controller)	5	89.3	1.2
Ciliated mesh/ Separate mesh Router	Designed according to number of tiers in 3D IC	70.1 + different according to number of tiers	0.7+0.1*n (n: number of tiers)
SPIN router	8	107.2	1.1
BFT router	6	80.9	0.9

C. Validation of 3D-Partition

In order to validate 3D-Partition, we implement the layouts of a 16-core processor in 45nm technology. The most popular tile-based design methodology in many-core processors is chosen in the experiment. Each tile consists of a Pentium™ class IA-32 core with L1 caches, a 256 KB private L2 cache [11-12] and a router. In order to compare the power and delay performance for various topologies, a combination of analytical models and Cadence Spectre simulation results are used to obtain power and delay numbers for the network components. These are then employed to obtain the power and delay parameters for the NoC simulation.

The processor is implemented in three partition strategies, 2D, 2-tier 3D and 4-tier 3D. We use NIRGAM to estimate the throughput and power consumption from the layouts and compare the results with those from 3D-Partition. We compare the results of 2-tier 3D and 4-tier 3D with the 2D implementation, and get the gain in throughput and savings in power consumption, which are illustrated in Table III. We observe that the throughput gain and power consumption trends for these designs predicted by 3D-Partition and the actual designs are similar. The reason why we validate the relative trends instead of absolute numbers is that the underlying technology parameters used by 45nm process by NIRGAM and the data we used in 3D-Partition for 45nm are different. This demonstrates that throughput and power consumption modeled by 3D-Partition coincide with NIRGAM simulation results.

TABLE II. NETWORK THROUGHPUT AND POWER CONSUMPTION FROM 3D-PARTITION AND NIRGAM OF 2-TIER 3D AND 4-TIER 3D COMPARED TO 2D IMPLEMENTATION

Type	3D-Partition 2-tier 3D vs 2D (%)	NIRGAM 2-tier 3D vs 2D (%)	3D-Partition 4-tier 3D vs 2D (%)	NIRGAM 4-tier 3D vs 2D (%)
Throughput gain	7.5	7.4	9.7	9.3
Power consumption saving	10.3	14	9.1	13.2

III. DESIGN SPACE EXPLORATION USING 3D-PARTITION

In the previous section, we've illustrated the compositive cost model used by 3D-Partition, and proved the feasibility of it by comparing the simulation results with those from NIRGAM. In this section, we explore various 3D architectures of different partition options of a many-core processor using 3D-Partition to choose the best tradeoff between fabrication cost, network throughput and power consumption. And the influence of weight in the cost model can also be seen here.

A. Experiment Object and Environment

Herein an 80-core processor is chosen as the experiment object. The core number is chosen among huge experiment data. From the standpoint of network performance, the performance of architecture will be best when a topology is regular and complete. For example, as for 3D mesh, the performance will be best when the core number is n3, and n2*m comes second. As for hyper octagon, the optimal core number should be (8+5*k+3*y)*n. As for Ciliated Mesh and Separate Mesh, the optimal core number should be n2*m. As for SPIN and BFT, the optimal core number should be 4*m. In all above m, n, k and y are integer. In order to fairly compare performance of those architectures, we must choose a proper core number to let the performance of them to be optimal or suboptimum.

The most popular tile-based design methodology in many-core processors is chosen in the experiment. Each tile consists of a Pentium™ class IA-32 core with L1 caches, a 256 KB private L2 cache [11-12] and a router. In order to compare the power and delay performance for various topologies, a combination of analytical models and Cadence Spectre simulation results are used to obtain power and delay numbers for the network components. These are then employed to obtain the power and delay parameters for the NoC simulation.

In order to acquire power characteristics, the routers of different 3D NoC architectures are modeled in VHDL. The width of the router links is 128 bits. Each port has four virtual channels and two-flit-deep virtual channel buffers. Then Synopsys Prime-Power is used to gather data of the energy dissipated by each router, the results of which is shown in Table I. And we compute energy dissipation of wires by estimate the capacitance, wire length and number of repeaters of wires.

In order to simulate the presented architectures, we use a flit-driven simulator with wormhole routing strategies. A synthetic traffic with a high degree of temporal and spatial communication locality is used here. Initially, the injection rates increase slowly until the network stabilize. In the next period of time throughput and power consumption are counted.

B. Architectures and Partition Options

Using 3D-Partition, we can do various simulations on the 80-core processor easily. It can be implemented in six 3D NoC architectures, 3D mesh, hyper octagon, ciliated mesh, separate mesh, SPIN and BFT, with various partition strategies. The user only need to input the number of tiers he wants to divide, choose an architecture from the six options, and select from homogeneous and heterogeneous partition, the software can automatically construct the 3D NoC and do the simulations. In this experiment, only six partition methods are chosen to show the functions of 3D-Partition.

C. Results

In the experiment, we use the 2-tier homogeneous 3D mesh NoC as the baseline. Using 3D-Partition, 3D mesh, ciliated mesh are implemented in 2-tier, 4-tier and 8-tier 3D ICs respectively. While separate mesh, SPIN and BFT are instantiated in 3-tier, 5-tier and 9-tier 3D ICs because all of the three architectures have one separate interconnect die. Hyper octagon is instantiated in 2-tier, 4-tier and 10-tier homogeneous and 2-tier, 4-tier and 8-tier heterogeneous 3D ICs because of the requirements of its special topology. All the data of the baseline also comes from simulation data.

Fig. 1 shows the ratio of fabrication cost and power consumption of all the six architectures under six partition strategies to those of the baseline and the ratio of throughput of baseline to all the architectures. The throughput part of equation is different because we want to cut back fabrication cost and power consumption but augment throughput. From the illustration we can see all aspects of relative compositive cost of all the architectures.

We analyze the data in Fig. 1 and get some conclusions which can help us to choose the best tradeoff between fabrication cost, throughput and power consumption. Some observations are listed as follows.

First, if we set the weight of fabrication cost, throughput and power consumption to be the same, which means Wc=Wt=Wp , the champion of compositive cost should be homogeneous 4-tier 3D mesh. In every aspect, from fabrication cost to performance, homogeneous 4-tier 3D mesh has good effect. But if weights were changed, the last results might vary. This will be decided by the actual applicative environments.

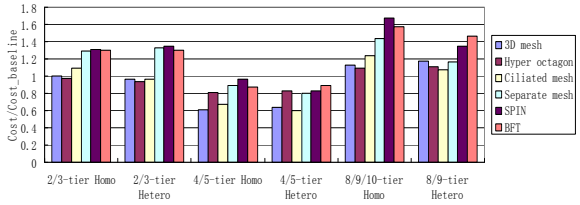
Second, under some circumstances, the performance of hyper octagon outperforms those of 3D mesh with the same partition method. But the expansion of hyper octagon in horizontal direction constrains the number of cores, which can only be 13, 18, 21, 26, 29, 34, 37, 40… If the partition method can't match the number, it will hinder the performance. So the hyper octagon is not flexible in scalability.

Third, ciliated mesh and separate mesh have relative stable performance whatever partition strategy is. The performance is better than some partition option of 3D mesh and worse than

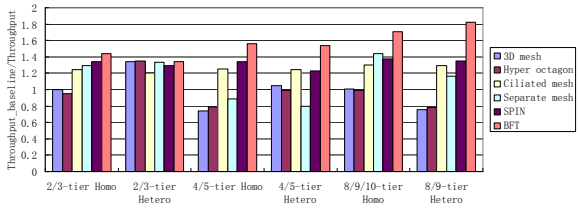
others. The fabrication cost of separate mesh is a little higher because of an extra interconnect die in 3D IC.

Fourth, tree-based architecture, SPIN and BFT, lag behind mesh-based architecture both in fabrication cost and performance.

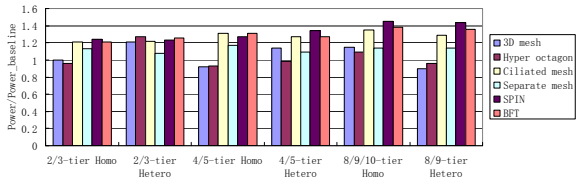
All the simulation data comes from 3D-Partition, a high-level exploration tool for 3D NoC. It can analysis relative compositive costs of six 3D NoC architectures under different partition strategies very quickly and help the users to choose the best tradeoff among various design options. The speed of the simulation tool is fast. And relative cost instead of absolute data is used to eliminate latent errors brought by different underlying technology parameters. So 3D-Partition is suitable for former design stage to choose from various designs to get a basic prototype.



(a) $\frac{fab\_cost}{fab\_cost_{baseline}}$



(b) $\frac{throughput_{baseline}}{throughput}$



(c) $\frac{power}{power_{baseline}}$

FIGURE I. RELATIVE FABRICATION COST, NETWORK THROUGHPUT AND CYCLE POWER CONSUMPTION OF ALL THE SIX ARCHITECTURES UNDER SIX PARTITION STRATEGIES.

IV. CONCLUSION

NoC has emerged as a revolutionary method for integrating a huge amount of embedded cores in a single die. Nevertheless the achievable performance benefit NoCs is constrained by the limitation of the metal wire. With technology scaling, depending on the material innovation can only extend the lifetime of conventional interconnect systems a few technology generations. According to the International Technology Roadmap for Semiconductors (ITRS), for the long run, new interconnect paradigms are required. The conventional 2D IC has limited layout choices, and consequently, it constrains the performance increment arising out of NoC architectures. 3D ICs are capable of achieving better performance, functionality, and packaging density compared to traditional planar ICs, and it solves the interconnect constrains of 2D IC. 3D NoC architectures can combine the benefits of NoC and 3D IC, and consequently offer an unprecedented performance gain.

To efficiently exploit the benefits of 3D technologies, design tools, and methodologies to support 3D NoC designs are imperative. In this paper, we present a high-level exploration tool for 3D NoC (3D-Partition), which explores the architectural design space of 3D NoC at the early design stage. 3D-Partition uses a compositive model of fabrication cost, network throughput and power consumption, supporting six 3D NoC architectures, 3D mesh, hyper octagon, ciliated mesh, separate mesh, generic fat tree (SPIN) and butterfly fat tree (BFT), to explore different 3D design options of 3D NoCs. It can evaluate more aspects and provide more options than existing 3D NoC exploration tools.

ACKNOWLEDGMENT

This work is supported by Bureau of Education of Guangzhou Municipality under Grant No. 1201421089.

REFERENCES

[1] A. Richard, et al., "Fast Design Space Exploration Environment Applied on NoC's for 3D-Stacked MPSoC's," in Architecture of Computing Systems (ARCS), 2010 23rd International Conference on, 2010, pp. 1-6.

[2] X. Menwang, et al., "Meshim: A high-level performance simulation platform for three-dimensional network-on-chip," in ASIC (ASICON), 2011 IEEE 9th International Conference on, 2011, pp. 349-352.

[3] O. Hammami, et al., "Design of 3D-IC for butterfly NOC based 64 PE-multicore: Analysis and design space exploration," in 2011 IEEE International 3D Systems Integration Conference, 3DIC 2011, January 31, 2012 - February 2, 2012, Osaka, Japan, 2011.

[4] X. Jiang, et al., "An efficient design algorithm for exploring flexible topologies in custom adaptive 3D NoCs for high performance and low power," in 2011 IEEE 9th International Conference on ASIC, ASICON 2011, October 25, 2011 - October 28, 2011, Xiamen, China, 2011, pp. 535-538.

[5] G. R. Price and A. Hum, Extension of covariance selection mathematics. London, 485-490.

[6] Y.-F. Tsai, et al., "Design Space Exploration for 3-D Cache," Very Large Scale Integration (VLSI) Systems, IEEE Transactions on, vol. 16, pp. 444-455, 2008.

[7] L. Meshkat, et al., "Requirements based system level risk modeling," in Reliability and Maintainability, 2004 Annual Symposium - RAMS, 2004, pp. 500-506.

[8] J. Wu and G. Wang, "Cost Evaluation on Reuse of Generic Network Service Dies in Three-Dimensional Integrated Circuits," Microelectronics Journal, vol. 44, pp. 152-162, 2013.

[9] P. P. Pande, et al., "Performance evaluation and design trade-offs for network-on-chip interconnect architectures," Computers, IEEE Transactions on, vol. 54, pp. 1025-1040, 2005.

[10] B. S. Feero and P. P. Pande, "Networks-on-Chip in a Three-Dimensional Environment: A Performance Evaluation," Computers, IEEE Transactions on, vol. 58, pp. 32-45, 2009.

[11] J. Howard, et al., "A 48-Core IA-32 Processor in 45 nm CMOS Using On-Die Message-Passing and DVFS for Performance and Power Scaling," Solid-State Circuits, IEEE Journal of, vol. 46, pp. 173-183, 2011.

[12] P. Salihundam, et al., "A 2 Tb/s 6×4 Mesh Network for a Single-Chip Cloud Computer With DVFS in 45 nm CMOS," Solid-State Circuits, IEEE Journal of, vol. 46, pp. 757-766, 2011

