Study on Dual-port RAM-based Image Capture and Storage

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Abstract. In the image acquisition system, acquisition speed affects the handling capacity of the entire system, Dual-port RAM for improving the acquisition rate plays a very important role. This paper presents a high-speed, low-cost dual-port buffer memory. The program is complex programmable logic (FPGA) circuit design implementation, simulation results show that the reservoir RAM reading and writing timing fully comply with the timing requirements, and Reading and writing results correctly.

Introduction

In the design and development of advanced instruments, such as real-time image acquisition, radar data acquisition, they will face the common problem, namely, the large amount of data, high speed transmission. In the high speed data acquisition and processing system, with the increase of the amount of the sample data and the increase of the information processing tasks, the request of data transmission is also more and more high. In the system or between modules without a high-speed data transmission interface, the data transmission can easily cause bottleneck or wait for a phenomenon, thus affecting the processing capability of the whole system of data. [1] In order to slow the speed of the acquisition module and the speed of the processor, it does not affect the speed of the data acquisition, but also to improve the utilization of the processor, In this paper, a dual port RAM is designed by using the static RAM which is rich in FPGA, which has the characteristics of high speed, large capacity, low cost, not only well solves the transmission congestion and Waiting phenomenon, but also improve the system of data acquisition and data processing ability, and validates the feasibility of the scheme through simulation.

Image acquisition module

The main function of image acquisition module is responsible for driving the image, and the image information collected by the sensor is stored in an external SDRAM chip in a certain format. Image acquisition and storage module structure diagram is shown in figure 1.

FPGA drive image sensor OV7670,which configuration process is achieved through the SCCB bus module, SCCB module sends configuration information to the image sensor, including the image output format, the size of the ranks, RGB gain, etc. Image sensor configuration is completed, which returns the collected digital image information to FPGA. Because it is the output of digital information, so we do not need to AD conversion and can be directly input into the FPGA chip.

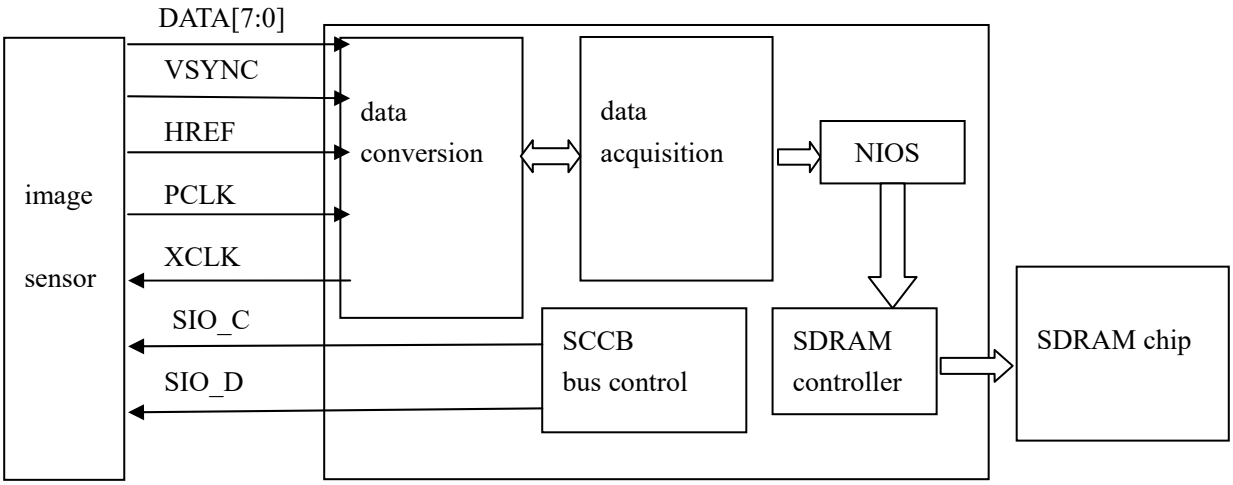

Fig. 1 the structure of image collect and storage module

Image acquisition process

Using HREF's OV7670 and VSYNC as the line and field control signal, The frequency of the output of the data bus we set to 25MHZ, which outputs a byte of valid data at the rising edge of each PCLK. We set the output format to RGB565, which is two bytes per pixel. In the storage of data, you can think of each of the two consecutive bytes of a pixel. HREF is the line reference output signal; HREF is the line reference output signal; When the HREF output is high, at this time it is the line of effective data; When the HREF output is low, the data is not valid. When VSYNC is low power, which repress the field blanking stage, the blanking stage of the data is invalid. The beginning of a new line of data transmission can be detected using the rising edge of the HREF signal. For each frame, we can be seen from Figure 3.4,that the starting point of each frame are in the beginning of the high level of three times the time, and can be achieved on the screen or refresh the SDRAM signal. [2]

As mentioned earlier, the image output format is RGB565, which is two bytes per pixel, In the preparation of storage, we have a pixel corresponding to a storage unit, which can save memory space, So we need to convert 8 adjacent two data into a 16 bit data and then store it, At this point we need add a sign of the number of judgments lable, which was set up, we could send a signal to write, When the write signal is received by the memory, we can store it.

The work rate of FPGA is much larger than the transmission rate of the sensor, If the kernel constantly monitor the arrival of the pixel data, this will greatly reduce the use of the kernel space, Because most of the time the kernel is waiting for the arrival of the data. In order to improve the use of the kernel space, this paper designed two dual port RAM, And there are independent write clock, write enable, write address and read clock, read enable, read address. Each RAM is able to store a row of pixel data, namely, the size of each RAM is 320*16=5120Bit, and is addressed in a word.

Design of dual port RAM control module

When a row of data is started, the data is always written to the empty RAM, At this time RAM full of sends data to the kernel, in the role of reading the clock, because the rate of reading data of the kernel is much greater than the rate of the sensor data, So when the start signal comes there is always an empty RAM waiting to receive data. Because of in this design,

the sensor data write clock is 10MHZ, the read clock is 50MHZ, kernel clock frequency is 130MHZ, which shows that the use of space can be greatly improved, and allows the kernel to perform other tasks, such as data processing or refresh display.

The dual port RAM control block diagram is shown in figure 2, This figure is a single dual port RAM control module, which consistent with the principle of another RAM control circuit.

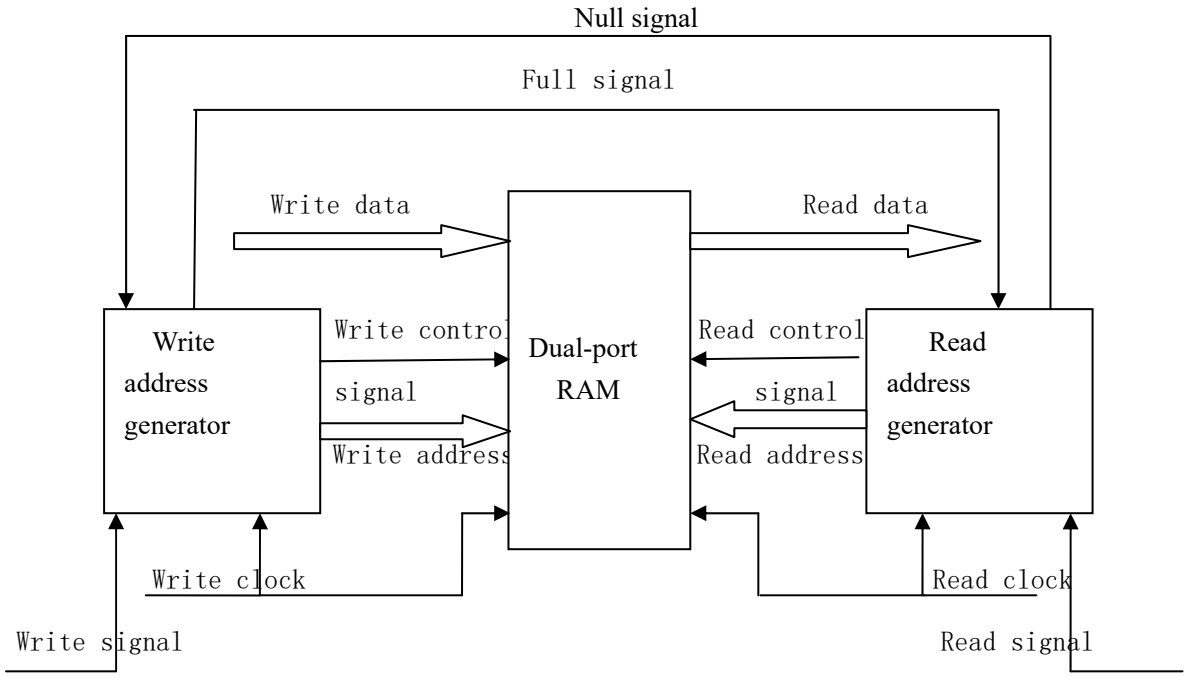

Fig. 2 the control flowsheet of double interface RAM

From the image above, The write address generator is judged by the null signal state RAM, according to the write clock signal and write signal generate write address, and full symbol generation logic is based on the size of the write address and the size of the dual port RAM, When the signal is valid, if you write the address +1=320, the memory is full, Then which outputs the corresponding full signal; Similarly, the read address generator is judged to be full RAM based on the full signal, according to the read signal and read the clock to produce read address, and null flag generating logic is based on the read address and the size of the dual port RAM, When the read signal is valid, if the read address +1=320, then which outputs the corresponding null signal. [3] The flow chart of the RAM image acquisition module based on two port is shown in figure 3.

After the arrival of the pixel data, firstly it through the DB8_16 module, which is designed to convert 8 adjacent two bit data into a 16 bit data, namely A pixel data, PCLK is pixel clock for sensor output, write is write signal, When the data meet the requirements at the write side there will be a rising edge, and perform as a write clock in RAM and address generator, namely data storage and address changes in the rising edge of write; Full as a sign of Full state of RAM, Full output high level when FIFO is full, When the soft nios2 detected the rising edge of full, which output read signal nios_read, and used to enable read clock rd_clk, Data output and address changes in the RAM and read address generator under the clock. Because the two RAM common one output and the clock, you need to set a two election 1 selector to connect the two RAM output and the Niso input or TFT32 input. [4]

The schematic diagram of the dual port RAM control module is shown in figure 4.

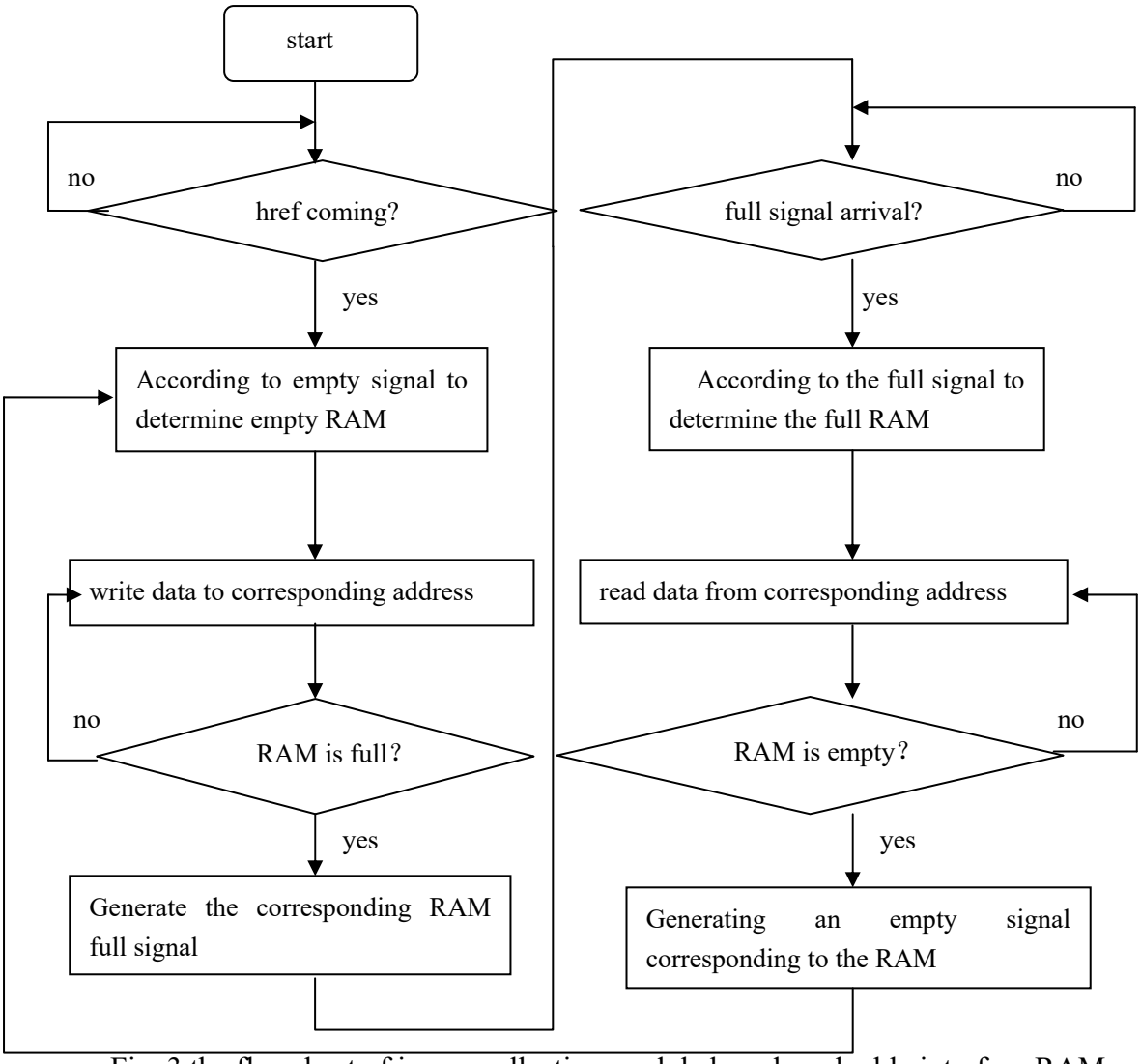

Fig. 3 the flowsheet of image collecting module based on double interface RAM

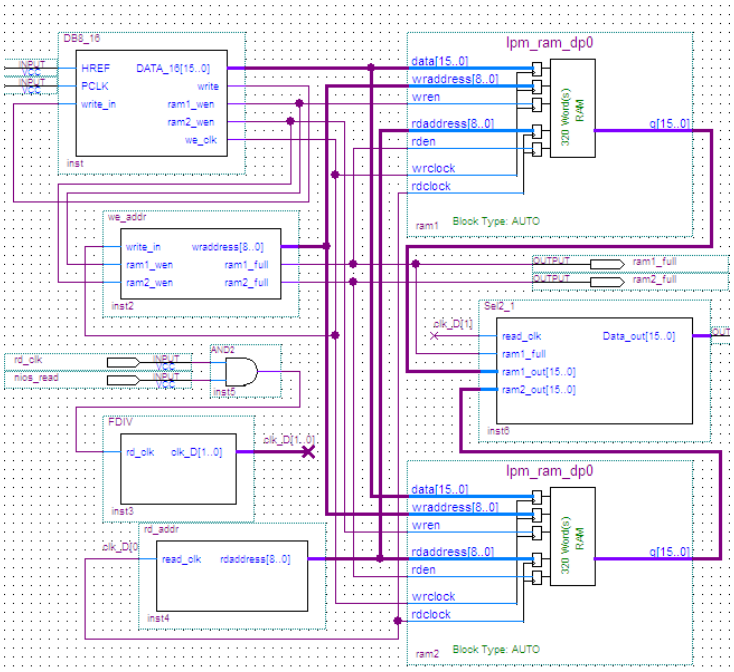

Fig. 4 the schematic diagram of double inface RAM control module

Simulation and implementation of dual port RAM control module

In order to verify the basic functions of the module can be achieved, we use the function of Quartrs II simulation, And in order to achieve the goal more easily, we change the size of the RAM block to 2 words, and artificially custom line signal HREF, pixel clock PCLK, read enable signal Nios_read and read clock rd_clk. the read clock and the size of the pixel clock we set is the same, Since the middle requires a 8 bit to 16 bit conversion module, and write the clock will be a corresponding reduction of times, so read the clock is faster than the write clock, which consistent with the premise of our design. Here we do not set the input of pixel data, but in the internal set a 8 bit variable, which do plus 1 of the operation with pixel clock PCLK.

Dual port RAM control module function simulation timing diagram is shown in figure 5.

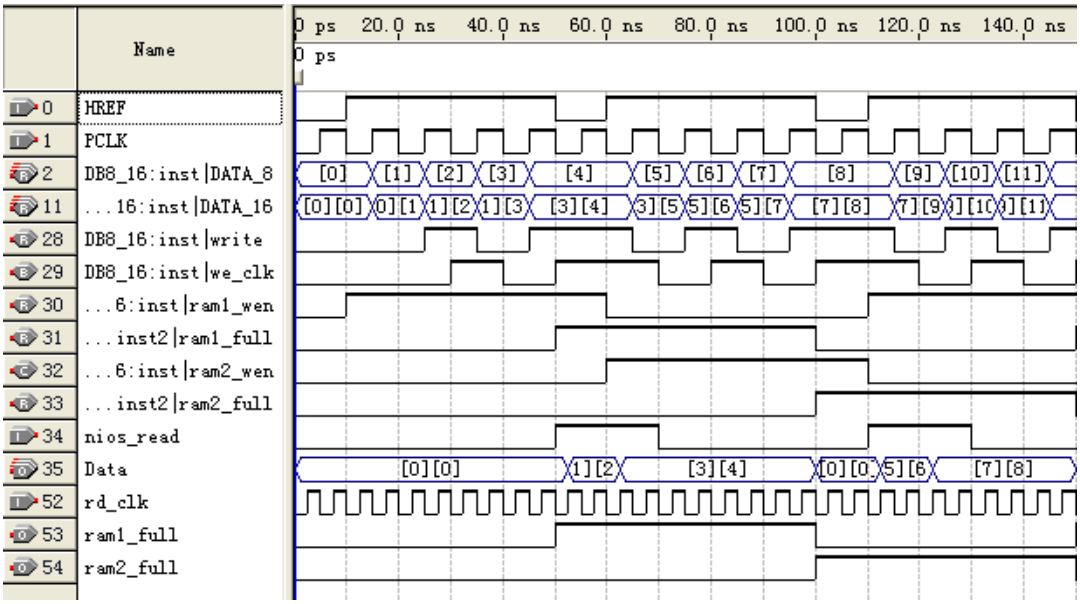

Fig. 5 the emulate timing of double interface RAM control module

Can be seen from the figure above, on the rising edge of HREF ram1 and ram2 read and write state is changed, and at the same time, the one and only ram is in the read or written form so as to realize the role of buffer. On the PCLK rising edge, internal variable DATA_8 adds 1, and every two PCLK cycles outputs a rising edge in the write port, and it is the data clock which RAM write clock and address generator clock comes with. In order to facilitate the simulation we set the size of the RAM to the size of 2 words, sonly 0x00, 0x01 two address store data. Because the write clock is slower than the data clock half a PCLK cycle, namely, when the data and address are ready, write the rising edge of the clock comes, which avoid empty situations. In the driver of the clock, the data for 0x00 and 0x01 addresses of ram1 are [12] and [34], Similarly the data for 0x00 and 0x01 addresses of ram2 are [56]and[78], So as to cycle down in turn. In the process of reading it produce two clocks D[0] and D[1] by the FDIV, and D[0] is two times as much as D[1], D[0] drive read clock and read address generator, D[1] mainly Sle2_1 by 2 selected 1 module, which can avoid the situation of reading empty, so that the data can arrive at the output in the correct order. From niso_read we can know read clock enable signal duration is very short, the data in another RAM can be read completely before a ram can be written, In this way, the kernel has more time to complete other tasks, which can improve the utilization of the kernel.

Conclusion

The dual port RAM proposed in this paper is realized by the static RAM with large capacity of the FPGA chip, which solves the problem of the slow speed of the acquisition module and the speed of the processor is not coordinated, and different sizes of RAM can be selected according to different capacity requirements. FPGA is rich in resources, and the selection is very flexible. In this scheme, the acquisition module and the processor at the same time do not access the same piece of RAM, which automatically switch according to the sign by the program. In this paper, the design of dual port RAM has the advantages of low cost and high throughput compared with the market independent dual port RAM low cost, and it can quickly realize the development of high speed and high speed equipment.

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Author introduction

Yuan Qinghui, male, Jining Shandong, Binzhou Polytechnic, mainly engaged in electrical automation engineering research and management.

