The Design of Direct Digital Synthesizer Based On Cordic Algorithm and FPGA Implementation

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Abstract. Currently, there are many methods that can implement direct digital synthesizer (DDS) including ROM look-up table method, Cordic algorithm and so on. Traditional DDS usually adopts the method of look-up table, which needs ROM to save a lot of waveform data. But the frequency resolution of DDS depends on how many ROM can save. Obviously the more data ROM can save, the better frequency resolution will be. Thus it takes the more ROM resources and the higher power dissipation while it gets the lower reliability and the slower conversion speed. However, Cordic algorithm use the method of iteration, which can generate high-resolution local oscillator signal through the shift, accumulation and subtraction operation. Compared with ROM look-up table, it reduces the occupation of the resources of ROM substantially. Therefore, this paper use Cordic algorithm to design DDS. At the same time, the Cordic algorithm is programmed into the FPGA device, which can generate sine and cosine waveform. The frequency and amplitude of waveform can be adjusted by the host computer. Then the desired waveform is simulated in Modelsim and Chipscope platform. As a result, the function of waveform is debugged and verified in hardware platform successfully.

Keywords: Cordic; DDS; FPGA; DAC; Modulation signal.

1. Introduction

Direct digital synthesizers are significant components in many digital communication systems. Firstly, a conventional DDS based on ROM lookup table is presented in this paper. The lookup table stores samples of a sinusoid. A digital integrator is used to generate a suitable phase argument that is mapped by the lookup table to the desired output waveform. Then, the principle of Cordic algorithm is deduced in detail. Because it can generate quadrature I/Q modulation signal using the circular rotation mode of Cordic algorithm. The amplitude and frequency of I/Q signal is adjusted by RS232 serial interface on the host computer. In addition, the I/Q signal can have optimal frequency resolution reaching 0.0466Hz.At the same time, the frequency accuracy of sine and cosine signal is better than 0.16%.

2. Conventional DDS from a phase to amplitude

The direct digital synthesizer based on ROM lookup table is shown in simplified form in Fig.1.It consists of phase accumulator and phase to amplitude converter.D1 is n bit increment register which can store digital phase increment temporaily.A1 is n bit full adder.D2 is n bit phase register.T1 is sine/cosine lookup table that converts phase to amplitude. When each f_{clk} comes, phase increment $\Delta\theta$ is transferred into D1.The output value of D1 is added to the output value of D2 by A1.The output value of phase accumulator is regarded as the address of lookup table. In advance, lookup table stores much value corresponding to the address of lookup table.

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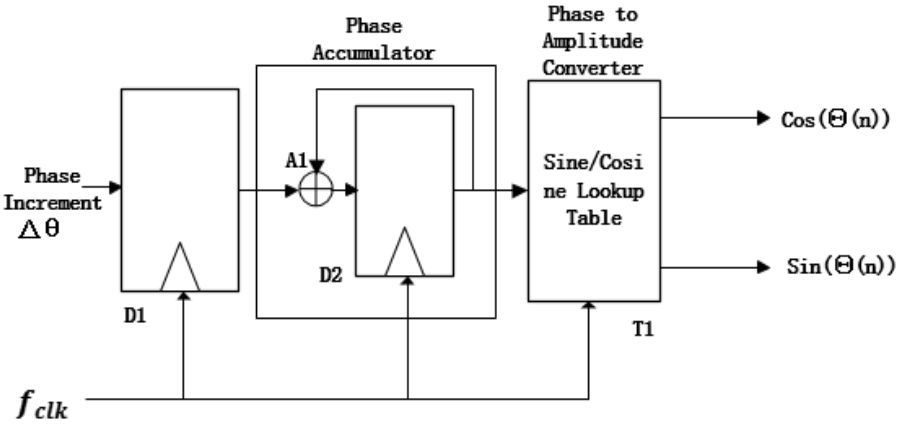

Fig.1 The block diagram Basing ROM lookup table

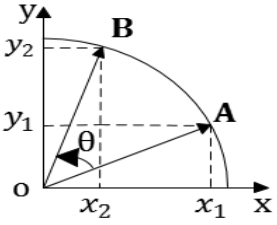

Fig.2 The rotation of circular coordinate system

The output frequency, f_{out},of the DDS waveform is a function of the system clock frequency, f_{clk}, the phase width, n, in the phase accumulator and the phase increment value Δθ.The output frequency is defined by:

$$f_{out} = \frac{f_{clk}\Delta\theta}{2^n} \tag{1}$$

The frequency resolution Δf is defined by:

$$\Delta f = \frac{f_{clk}}{2^n} \tag{2}$$

Where f_{clk} is clock frequency, n is number of bits employed in the phase accumulator? Δf Is found by setting$\Delta\theta = 1$.

From the above formula, it can be seen that the value of n is desired to increase or the value of f_{clk} is desired to decrease if high frequency resolution is acquired. However, f_{clk} mustn't be small arbitrarily because of Nyquist sampling theorem:

$$f_{clk} \geq 2 f_{out} \tag{3}$$

Thus the value of n is increased dramatically for high frequency resolution. But it leads ROM lookup table to store more data. It is obvious that it has many disadvantages of higher power dissipation, lower reliability and the slower conversion speed. As a result, Cordic algorithm is used to design DDS for generating I/Q modulation signal.

3. The principle of DDS basing on Cordic algorithm

The point A(x1, y1) to point B(x2, y2) is rotated by θ degrees on the x-y plane in Fig.2 .It is shown by the following formula:

$$\begin{bmatrix} x_2 \\ y_2 \end{bmatrix} = \begin{bmatrix} cos\theta & -sin\theta \\ sin\theta & cos\theta \end{bmatrix} \begin{bmatrix} x_1 \\ y_1 \end{bmatrix} \tag{4}$$

If the right section is divided by cosθ in equation (4) and cosθ the common factor is not considered, the following pseudo rotate equation is obtained:

$$\begin{aligned} x_2^{'} &= x_1 - y_1 tan\theta \\ y_2^{'} &= y_1 + x_1 tan\theta \end{aligned} \tag{5}$$

The angle of rotation is right in pseudo rotate equation, but the amplitude of x and y is$1/cos\theta$of previous value. Because it is difficult to figure up $\tan\theta$ in the computer, $\tan\theta$ can be set to equal 2^{-i}($\tan\theta = 2^{-i}$).It's not hard to see that a certain number multiplied by $\tan\theta$ would become the

shifting of itself. In this way, pseudo rotate can be finished by a series of iteration factor i of continuous small angle. The equation of Cordic iteration algorithm can be described by:

$$\begin{cases} x_{i+1} = x_i - \delta_i y_i 2^{-i} \\ y_{i+1} = y_i + \delta_i x_i 2^{-i} \\ z_{i+1} = z_i - \delta_i \theta_i \end{cases}, \text{ where } \theta_i = \begin{cases} \arctan 2^{-i}, m = 1 \\ 2^i, m = 0 \\ \arctan h 2^{-i}, m = -1 \end{cases},$$

where δ_i is the direction of rotation, z_i is the sum of rotation angle.

In the model of rotation, the equation of iteration become the following formula by n iteration:

$$\begin{cases} x_{i+1} = \frac{1}{K_n}(x_0 \cos z_0 - y_0 \sin z_0) \\ y_{i+1} = \frac{1}{K_n}(y_0 \cos z_0 - x_0 \sin z_0) \\ z_{i+1} = 0 \end{cases}, \text{ where } K_n = \prod_n \frac{1}{\cos\theta^{(i)}} = \prod_n \sqrt{1 + 2^{(-2i)}}$$

When the module of Cordic is used to generate waveform, so $x_0 = K_n, y_0 = 0$， $z_0 = \alpha$,the following equation of I/Q modulation waveform are obtained:

$$\begin{cases} x_n = \cos\varphi \\ y_n = \sin\varphi \\ z_n = 0 \end{cases} \quad (6)$$

4. The hardware system of FPGA implementation

4.1 The hardware components of the waveform generating system

The components of hardware include FPGA minimum system board, high speed and precision DA circuit board, upper computer and low pass filter in Fig 3. The Cordic algorithm is programmed into the FPGA minium system board which can generat digital sine and cosine signal. Then, the signal is entered into the D/A-converter, which gets an analog sine and cosine waveform. The high frequency sampling components is removed by the low pass filter to get a pure sine wave output.

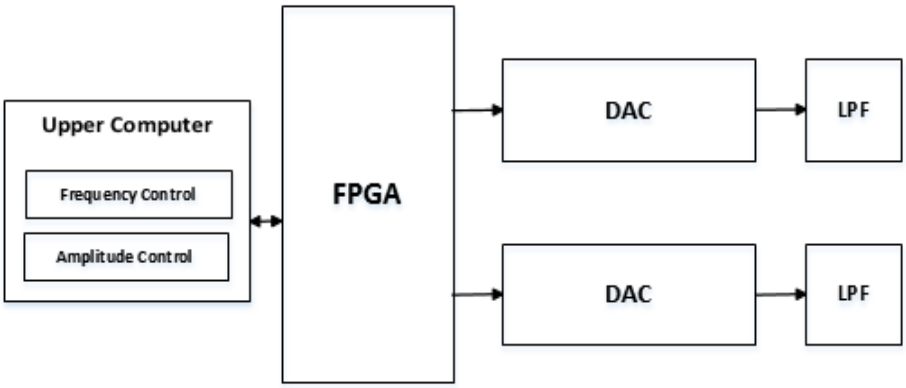

Fig.3 The block diagram of hardware system

Fig.4 The platform of hardware experiment

4.2 The design of communication interface

The system communicates with the upper computer by the RS-232 interface. Through the serial communication, the upper computer can set the frequency and amplitude.

5. Simulation and experiment results

The sine and cosine waveform are simulated about timing in Modelsim SE platform in Figure 5.It can be seen that the first waveform is cosinusoid and the second waveform is sinusoid. It is shown that the quadrature modulation signal correspond with the principle of Cordic algorithm. Chipscope Pro is set, which complies with the regulations. The cosine waveform is simulated online in Figure 6.

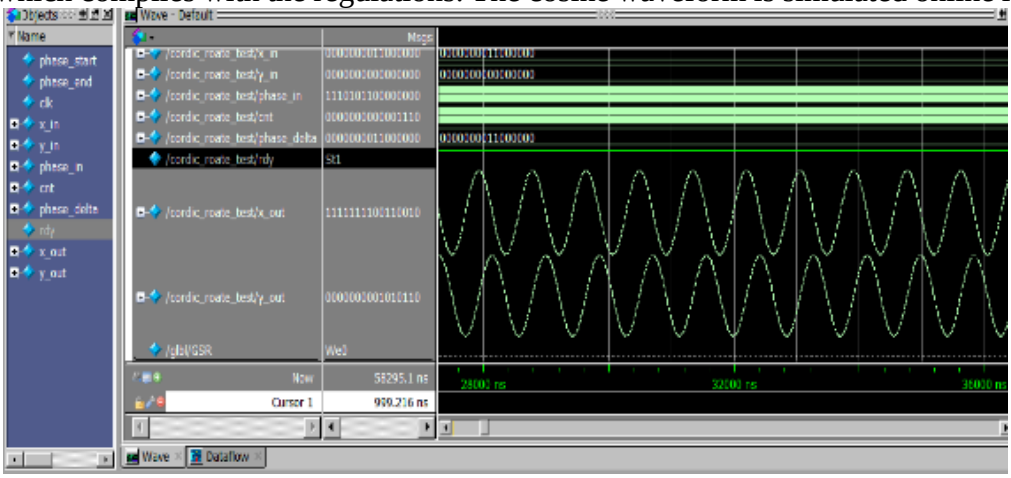

Fig.5 The waveform in Modelsim simulation platform

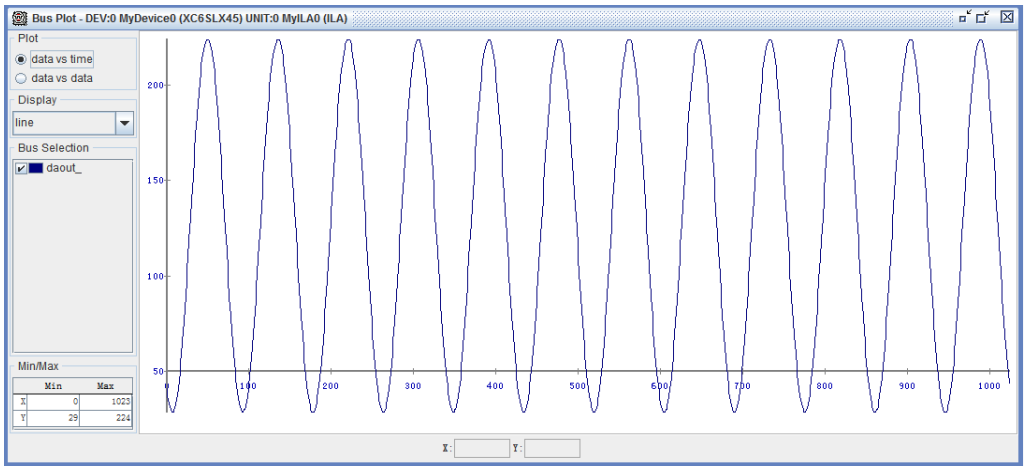

Fig.6 The waveform in Chipscope platform

In addition, the program of DDS module is downloaded to FPGA minimum system board. The signal is entered into the D/A-converter, which is displayed on oscilloscope in Figure 7. It is clearly obtained that the frequency of cosine signal is 585 KHz from Figure 7.The frequency equation of output signal is described:

$$f = \frac{F \times dphase}{2} \tag{7}$$

Where F is clk frequency of FPGA at work, dphase is decimalism of phase step.

The frequency of output signal that can be calculated is 585.9 KHz. The frequency accuracy of cosine signal is:

$$\varepsilon = \frac{585.9 - 585}{585.9} \times 100\% = 0.15\% \tag{8}$$

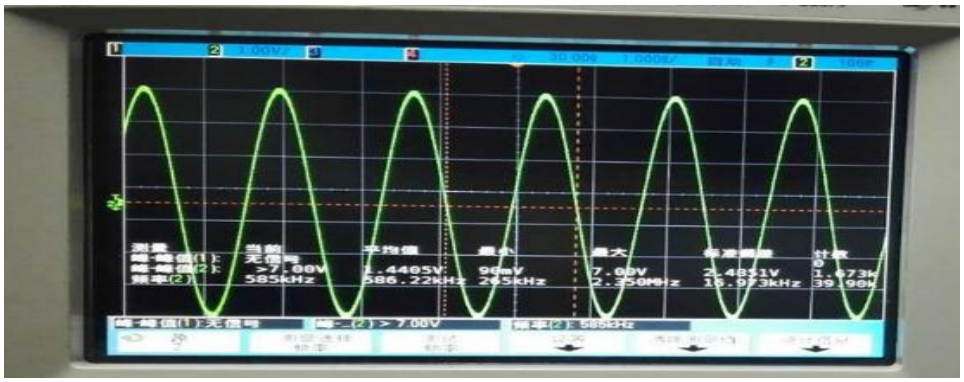

Fig.7 The modulation signal waveform in oscilloscope

6. Conclusion

In this paper, DDS basing on Cordic algorithm can generate quadrature modulation sine/cosine signal. The modulation signal can have optimal frequency resolution reaching 0.0466Hz and the frequency accuracy of signal is better than 0.16%.

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