Design of High Speed Sampling Clock Based on LMX2531

Bing Zhou [a], Zhengsheng Li [a] and Hao Chen [b]

Xi'an Research Institute of High Technology, Xi'an 710025, China

[a]1194791524@qq.com, [b]2282749486@qq.com

Abstract. The LMX2531 is a low power, high performance frequency synthesizer system which includes a fully integrated delta-sigma PLL and VCO with fully integrated tank circuit. The third and fourth poles are also integrated and also adjustable. Also included are integrated ultra-low noise and high precision LDOs for the PLL and VCO which give higher supply noise immunity and also more consistent performance. When combined with a high quality reference oscillator, the LMX2531 generates very stable, low noise local oscillator signals for up and down conversion in wireless communication devices. In the system, the LMX2531 is controlled by FPGA. It outputs a 1500MHz clock signal through programmed eleven 24-bit registers with Verilog HDL. The signal is very suitable to be used as the sampling clock of ADC in high speed acquisition system for it has the characteristics of low jitter and high stability.

Keywords: LMX2531; Sampling clock; Verilog HDL; Low jitter.

1. Introduction

With the development of electronic technology, data acquisition technology has been widely used in digital communication, image processing, military applications and other fields, and it is developing toward the high sampling rate and high precision. In the high speed data acquisition system, the analog to digital converter (ADC) is the key part of the sampling system, which directly affects the quality of the sampled signal. Sampling clock as an important indicator of the performance of ADC, its signal quality directly affects the sampling quality. In the high speed ADC circuit, the sampling clock jitter will have an important impact on the data acquisition, which will make the SNR of the ADC conversion circuit decline and decrease the effective bit of the sampled data. So it is very important to design a low jitter sampling clock for improving the quality of data acquisition. In the system, it uses the lmx2531 chip as the key part and combined with FPGA as the control core, designs a sampling rate up to 1500MHz clock signal. The sampling clock has the advantages of high integration, convenient debugging, programmable and so on, which is very suitable for high-speed ADC sampling clock.

2. Introduction of the LMX2531 chip

The LMX2531 is a low power, high performance frequency synthesizer system which includes a fully integrated delta-sigma PLL and VCO with fully integrated tank circuit. The third and fourth poles are also integrated and also adjustable. Also included are integrated ultra-low noise and high precision LDOs for the PLL and VCO which give higher supply noise immunity and also more consistent performance. When combined with a high quality reference oscillator, the LMX2531 generates very stable, low noise local oscillator signals for up and down conversion in wireless communication devices. The LMX2531 is a monolithic integrated circuit, fabricated in an advanced BiCMOS process. There are several different versions of this product in order to accommodate different frequency bands. Device programming is facilitated using a three-wire MICROWIRE Interface that can operate down to 1.8 volts. Supply voltage range is 2.8 to 3.2 Volts. The LMX2531 is available in a 36 pin 6x6x0.8 mm WQFN Package [1]. The internal function of LMX2531 is shown in Figure 1.
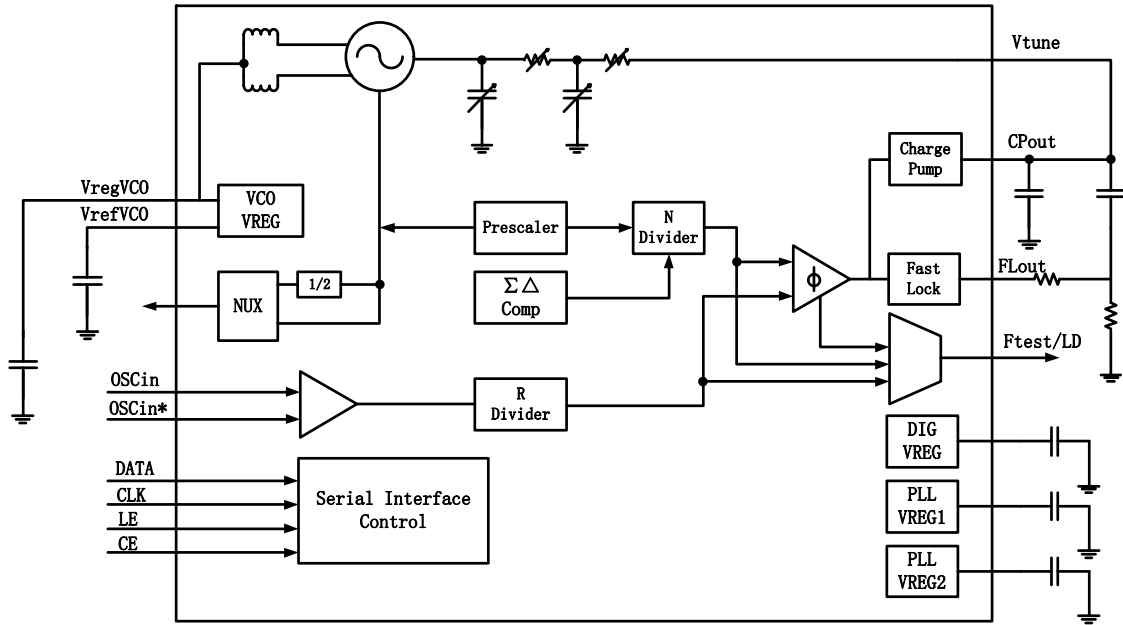
Fig.1 LMX2531 function block diagram

The LMX2531 mainly consists of frequency detector, loop filter, voltage controlled oscillator, frequency calibration circuit of voltage controlled oscillator and serial interface control circuit. When the external oscillator frequency is fixed (crystal frequency must be 5~80MHz), voltage controlled oscillator output and fout is determined by Prescaler, N-Divider, R-Divider and MUX. [2]

External controller controls the LMX2531 chip output clock signal by programming through the serial interface DATA, CLK and LE. LMX2531 has a total of 14 24-bit registers, including R10, R11 and R13 are the hidden shift registers, and R0, R1, R2, R3, R4, R5, R6, R7, R8, R9 and R12 are the programmable shift registers. The 24 bit shift register is used as a temporary register, which is used to program the register on the chip indirectly. The shift register is composed of two parts: the data area and the address area. The last 4 bits of the register form the address area, which is used to identify the internal register address, and the remaining 20 bits form the data area. Constitute. When LE is low, data go into the shift register at the rising edge of serial clock signal; when the LE becomes high, the data in the data area is sent into the internal register. The register initialization order must be: R5 (init1) →R5 (init2) →R5 (init3) →R12→R9→R8→R7→R6→R4→R3→R2→R1→R0, and in order to ensure the normal operation of the chip LDO, the write time between R5 (init3) and R1 shall not be less than 10ms. The timing diagram of the LMX2531 register is shown in Figure 2 below.
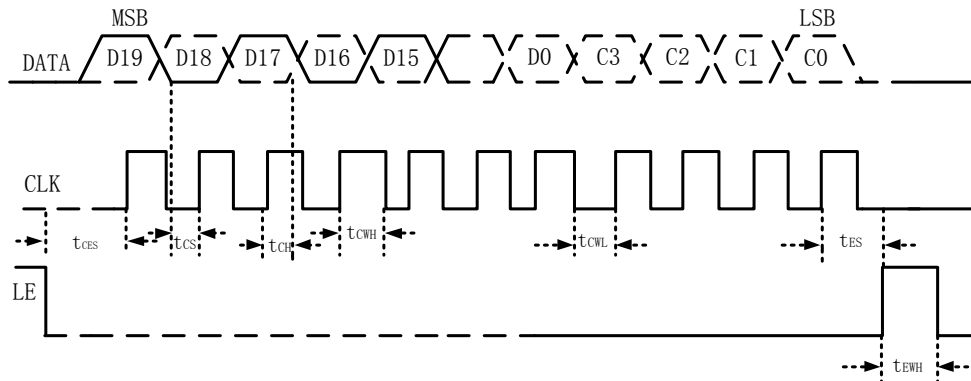

Fig. 2 LMX2531 register timing diagram

The formula for calculating the output frequency of LMX2531 is:

$$f_{vco} = f_{oscin} \times N / R \qquad N = N_{Integer} + N_{Fractional}$$

Type: f_{oscin} is external crystal oscillator frequency, and R is frequency division coefficient; the preferable value is 1, 2, 4, 8, 16 and 32. $N_{Integer}$ is the integral part of output frequency divided by

comparison frequency; $N_{Fractional}$ is the fractional part of output frequency divided by comparison frequency.

3. Hardware circuit design

In this paper, it needs to design a sampling frequency of 1500MHz clock signal, and the selection of the core chip is LMX2531LQ1515E. In the system, the LMX2531 is controlled by FPGA. It outputs a 1500MHz clock signal through programmed eleven 24-bit registers with Verilog HDL. The concrete control circuit is shown in figure 3.
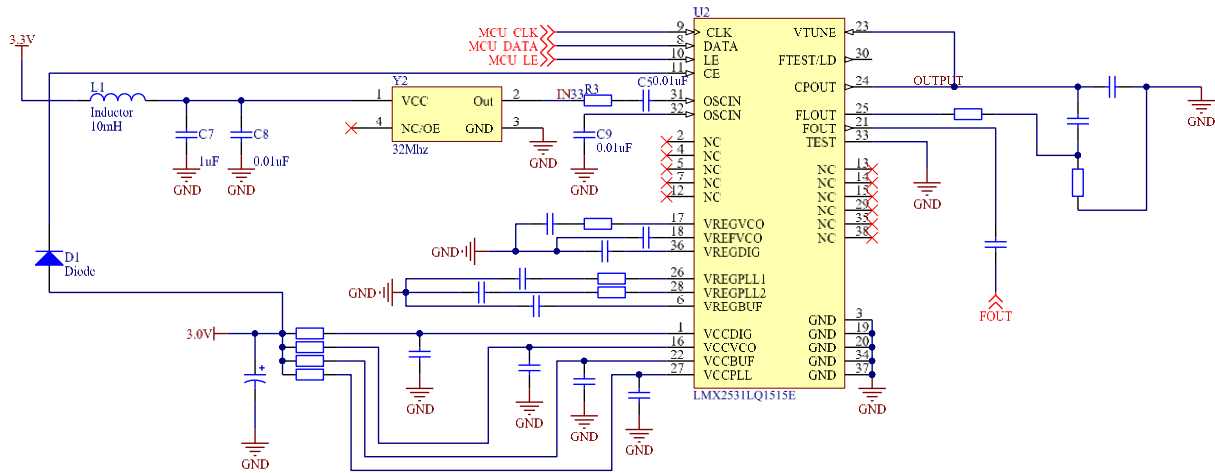

Fig. 3 LMX2531 hardware circuit

4. Software programming control

In this system, when the external input is 50MHz active crystal, according to the output frequency calculation formula, then the frequency division coefficient is 2, and the value of the N register is 60, the sampling clock of the output 1500MHz can be obtained. At the same time, according to the value of R and N, combined with the LMX2531 chip data, we can determine the value of 24 11 bit shift register. The system control LMX2531 shift register assignment with Verilog HDL language and then through the serial port to transfer data to the chip inside the 24 11 bit shift register to control the LMX2531 output 1500MHz clock signal. In this design, by changing the model of the LMX2531 chip and the value of the shift register, it can output the sampling clock signal with different frequency, and the frequency range of the signal can be obtained: 553~3132MHz. The core program is shown below.

```
Register assignment:
parameter [23:0] R5_1    = 24'b1000_0100_0000_0000_0000_0101;
parameter [23:0] R5_2    = 24'b1000_0000_0000_0000_0000_0101;
…
parameter [23:0] R2    = 24'b0100_0000_0000_0100_0001_0010;
parameter [23:0] R1    = 24'b0011_1110_0000_0000_0000_0001;
parameter [23:0] R0    = 24'b1001_0110_0000_0000_0000_0000;
Main program:
always@(negedge CLK_IN)
begin
    if(!CONFIG_EN)
            begin
                    j<=0;CONFIG_LE<=1;i<=4'b0;        CONFIG_SDATA<=0;
            end
    else
            begin
                    if(i>12)
```

```verilog
                            begin
                            CONFIG_SDATA<=0;CONFIG_LE <= 1;j<=0;
                            end
                else
                            if(j<=23)
                                    begin
                                    CONFIG_SDATA <= Temp_reg[23-j];j <= j+1'b1;
CONFIG_LE <= 0;
                                    end
                            else if(j<29)
                                    begin
                                    CONFIG_LE<=1; j <= j+1'b1; CONFIG_SDATA<=0;
                                    end
                                else if(j>=29)
                                            begin
                                            i<=i+1'b1;j<=0;CONFIG_LE<=1;
                                            end
            end
end
always@(posedge CLK_IN)
begin
        case(i)
                4'b0000:        Temp_reg=R5_1;
                4'b0001:        Temp_reg=R5_2;
                …
                4'b1100:        Temp_reg=R0;
                default:        Temp_reg=24'b0;
        endcase
end
```

5. LMX2531 output phase noise simulation

Clock Design Tool is the NS Company developed a clock design simulation tool, using it can easily design a low jitter and stability of the sampling clock and the phase noise can be simulated. Design is divided into three steps. The first step, select a single phase locked loop clock chip, and set the reference input clock and the output clock frequency. In the design, it selects the 50MHz reference clock and sets the output frequency to 1500MHz. The second step, choose LMX2531LQ1515E as the clock chip in the choice of the clock chip. Third, choose the correct parameter configuration. The obtained phase noise simulation diagram is shown in figure 4.
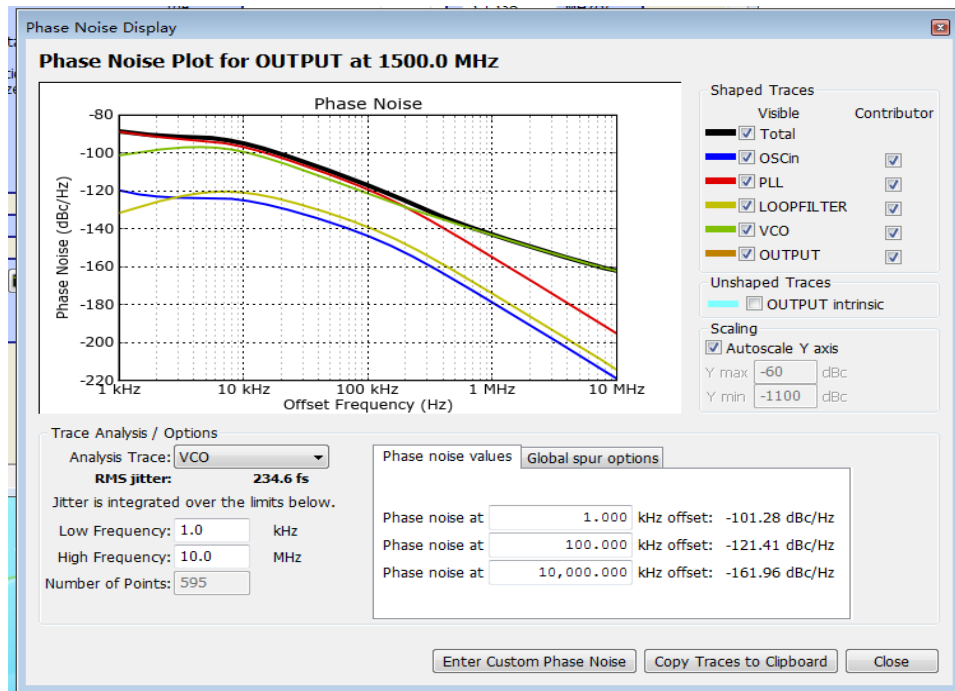
Fig. 4 phase noise (*f*=1500MHz)

By observing Figure 4, it can be known that when the output frequency is 1500MHz, the phase noise is -100dBc/Hz at the value of 1 kHz, -121.41dBc/Hz at the value of 100 kHz, -161.96dBc/Hz at the value of 10MHz. It can be seen that the power of the output signal is concentrated in 1500MHz, so it can be known that the clock signal has a high signal to noise ratio, and it can output low jitter and stable 1500 MHz clock signal.

6. Summary

In this paper, it introduces the internal structure and working principle of the LMX2531 chip and use FPGA control LMX2531. Through written the Verilog HDL language, it can control the internal registers on the LMX2531 chip to output of the clock signal 1500MHz. Finally, the phase noise simulation of the design was carried out by Design Tool Clock software. According to the simulation results, it can be shown that the output clock signal has low jitter and stable characteristics, which is very suitable to be used in high speed ADC sampling clock, and it has important significance for the design of advanced mathematics acquisition system.

References

[1]. LMX2531 Data Sheet [Z].

[2]. Jun Yang, Yan Jia, Zibin Wang, et al. Design of high frequency clock generation circuit of DSO. Chinese Journal of Scientific Instrument. (2007) No.S1, p.18-20.

[3]. Lan Mu. Design of transmitting circuit of UHD RFID reader based on LMX2531. Electronic Design Engineering. (2013) No.21, p.175-177.

[4]. Lin Tong. The Design of High-speed Programed Multi-clock Circuit System. Electronic Engineering & Product World. (2012) No.07, p.43-45.

[5]. Xueping Zhang, Ziquan Tong, Lijun Ren, et al. Clock design in high speed data acquisition. Foreign Electronic Measurement Technology. (2006) No.9, p.12-15.