Research of Multiple Channels Synchronous Wideband LFM Signal Generation Technology

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Abstract. The overall design of multiple channels synchronous wideband LFM signal generation technology takes the chip AD9914 as the core. It utilizes the method of Direct Digital Frequency Synthesis (DDS) to generate LFM signal. And it realizes the system control by FPGA device. Multiple channels double wave-band synchronous wideband LFM signal is generated by multiple AD9914 chips working at the same state. Then mixer up-convert the synchronous signal to the target frequency band, which can meet the requirement of the whole system. This design has the ability to expand to multiple wave-band, which lays a good foundation for future research.

Keywords: Multiple channels; Synchronization; Broad band LFM; AD9914.

1. Introduction

The multiple-channel signal source uses analog method and digital method to realize phase control. The analog method divides single signal into multiple signals, tuning the phase of the signal by the method of time delay of each signal. The phase adjustment circuit of this method is very complex, not conducive to testing the miniaturization and automation of the system [1]. And the circuit of digital method is simple, because the system need the infinite number of quantization bits analog to express the analog signals. In fact, the number of quantization bits is limited by a variety of factors. It is inevitable to draw in the quantization errors [2, 3]. With the development of the theory of digital signal and the technology of integrated circuit, great changes have occurred in the field of frequency synthesis technology. Since 1970s, the direct digital frequency synthesis technology has been developed. Compared to the traditional frequency synthesis technology, DDS technology has a lot of characteristics such as higher frequency resolution, shorter frequency switching time, continuous phase change and easy to realize a variety of modulation methods. The frequency of current high-speed DDS clock is up to 3.5 GHz. And bandwidth of its output signal is more than 1 GHz. The chip has many advantages, such as single, superior performance, easy to use, small size and low power consumption. Thus, DDS is very suitable for this study [4].

According to the performance of the current AD9914 DDS chip, its maximum frequency of the internal clock of is 3.5 GHz by the DDS signal generated method. And the output signal frequency can range from 0 GHz to 1.4 GHz. Therefore, this system can directly generate P band signal, or X band signal can be generated via mixer. The principle of the system realization is as figure 1:

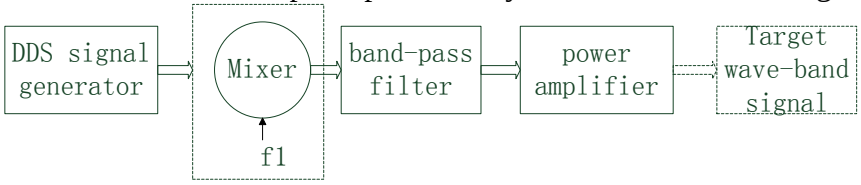

Fig.1 Principle of the system

The AD9914 chip is set to generate signals in the model of Digital Ramp Generator (DRG). In the DRG mode, the control parameters of the modulated output signal is modulated by the digital ramp generator (DRG) directly. And through the DRG module, it can provide upper and lower frequency and the rising slope. Thus it can produce 1 GHz bandwidth signal by this method. As the BPF transition zone holds a certain width, this study choose to produce broadband signal range from 0.2 GHz to 1.2 GHz. By this way, we can produce broadband signal range from 0.2 GHz to 1.2 GHz via

the DRG module. Then we can get the target X band signal through mixer and band-pass filter. The P band signal can be produced by DDS chip with the DRG module programming, which is range from 0.5 GHz to 1.0 GHz.

Double wave-band function has become the development trend of the battlefield reconnaissance radar system. Double wave-band radar can also provide multiple spectral characteristics of the target, which is conducive to the discovery of uncovered targets and hidden targets. The combination of general and detailed investigation and the combination of static and moving target detection are conducive to fully grasp the situation of battlefield.

With the background of small-sized digital array radar, the research of multiple channels double wave-band synchronous wideband LFM signal generation technology aims to find a kind of multiple-channel synchronous wideband LFM signal generation technology, which can solute the problem of wideband signal synchronization. At the same time, it contains the ability to transmit multiple wave-band signals, while having the characteristics of small-size, low power consumption and low cost. Then it is suitable for the application of digital array.

2. DDS signal generation module

According to the working and signal output requirement of DDS module, the designed hardware system of the 8 channel synchronous signal source (8-DDS) module is shown in Figure 2:

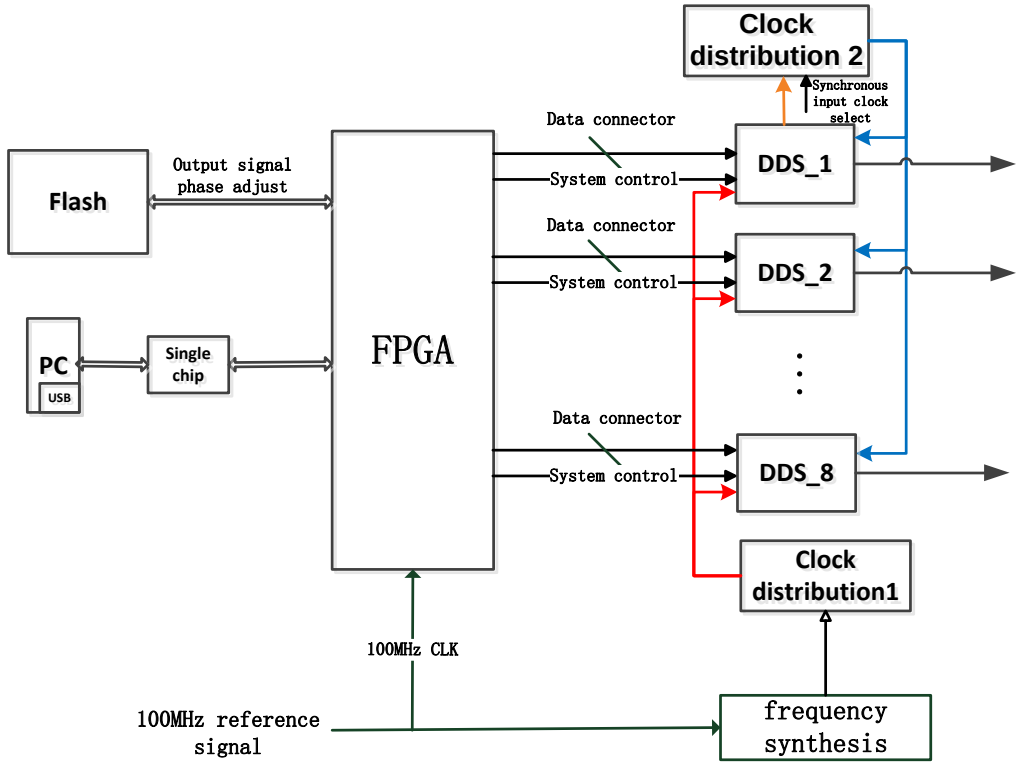

Fig. 2 8-DDS module hardware design

This system is divided into three functional units: control unit, signal generation unit, DDS synchronization unit.

(1) The DDS control unit is fulfilled by FPGA and FLASH. The clock of FPGA is given by the reference signal. And FPGA can control the system and data programming of DDS chip. The main function of FLASH is to store procedures. Through debugging and result analysis, the phase adjustment of the output signal is storage to the FLASH with the programming method to make the DDS chip output signal synchronous with other work.

(2) Signal generation unit is constitute by 8 DDS chips, shown in Figure 1, whose main function is to produce the required frequency linear modulation signal.

(3) DDS synchronization unit aims to achieve eight DDS strict synchronous state. The system needs to provide eight signals of synchronistical SYSCLK signal, SYNC_IN and IO_UPDATE

signals. These signals is respectively given by the clock distribution chip 1, clock distribution chip 2 and FPGA control.

3. Synchronization

3.1 Synchronization Principle

In order to obtain the multi-channel synchronous signal, we take focus on the synchronization method of DDS chip. The basic working process of AD9914 is transmit the external data to the internal registers by the IO_UPDATE signal. It changes the working state of AD9914. So the synchronous achievement needs internal state match and the state transition synchronization of the AD9914 chip's and it needs external IO_UPDATE signal synchronization. But AD9914 internal state synchronization needs to meet two conditions: the clock state matching and SYNC_CLK synchronization. DDS chip can use the internal synchronous reference chip (SYNC_IN) input clock signal to adjust the system clock state within the DDS. The synchronous SYNC_IN signal can adjust the working condition of DDS synchronization to a certain clock. By this, it can achieve the phase control and the status of the DDS synchronization signal. In the working condition of synchronous DDS, synchronous DDS chip can output the synchronous signal. Therefore, the output signal of multiple-channel synchronous DDS chip needs synchronous input clock signal which is provided by the internal clock signal and the external trigger signal. In the input clock state matching conditions, this system only need to correctly configure the clock the DDS signal and the trigger signal.

We should note that the synchronous reference frequency signal is 1/N frequency division of the internal clock signal. It requires the DDS chip should work according to the rise edge of 1/N inside clock frequency signals when the equipment startup. When the inside of each frequency in the N rising edge, we have to choose a rising edge as the initial phase. And the output of a synchronous signal is specified on a rising edge. And the status changes of the DDS is also affected by SYNC_CLK and I/O_UPDATE. Thus, in order to achieve multiple AD9914 chips working state synchronization, it needs meet three conditions:

(1) Input clock state matching and state transition synchronization.

(2) SYNC_IN signal synchronization.

(3) Trigger the I/O_UPDATE signal at the same time.

AD9914 synchronization problem is equal to realize three sets of signals. We can obtained the three conditions by certain conditions. For the first condition, we can choose stable clock distribution chip and the same length line to ensure the system clock state of AD9914 and the state transition synchronization. For the second condition, the system trigger the synchronous I/O_UPDATE signal by FPGA to ensure that all AD9914 chips receive synchronous I/O_UPDATE signal. There are how we get the synchronous SYNC_CLK signal.

The AD9914 chip set a SYNC_CLK pin which is used to multiple chip synchronization in multiple synchronization module. It is convenient to monitor the SYNC_CLK signal for the user. The basic process of multiple chip synchronization module is the main AD9914 output signal(SYSCLK 384 frequency division) send through the SYNC_OUT pin by buffer allocation (for example, through the signal line, with a clock distribution chip transmission) to each AD9914 (including main chip) SYNC_IN pins. The AD9914 chips receive the reference SYNC_IN signals to adjust their working condition. And the system can get the synchronous SYNC_CLK signal.

3.2 Synchronous circuit design

According to the project target and project requirements, the design of the clock as shown in figure 3:

In Figure 3, the clock distribution 1 output REF_CLK signal to the AD9914. It requires the transmission lines are equal to provide synchronous the REF_CLK clock signal. Clock distribution chip 2 output the SYNC_IN signal to the AD9914 which use the equal length line. The distribution chip 2 transmit the SYNC_OUT signal from the main DDS chip to all DDS chips. It makes the AD9914 synchronous of REF_CLK and SYNC_IN signals. Thus, the AD9914 operates in a

synchronous state. To enable FPGA to provide I/O_UPDATE signal synchronization, we can obtain multiple output synchronization.

The external circuit provide 100MHz reference signal to the system as the clock signal. PLL increase the 100MHz clock signal up to 3.5GHz through the internal VCO function. And the signal act as the input clock signal clock of the clock distribution chip 1. The clock distribution chip 1 distributes one clock clock signal into 8 output signals that are synchronous. The clock distribution chip 1 outputs 8 channels clock signal to the DDS chip as DDS working clock.

At the right end of the DDS chip, DDS_M chip's SYNC_OUT output SYNC_OUT signal which is used to complete synchronization. This signal' frequency is 9.1MHz.. So clock distribution chip 2 distributes this signal to the 8 AD9914 chip, as SYNC_IN signal.

The line distance from the clock distribution chip 1 output signal to AD9914 chips is equal to complete the synchronization requirements. And the line distance from clock distribution chip to SYNC_IN also has the same require. This will complete the system clock supply.

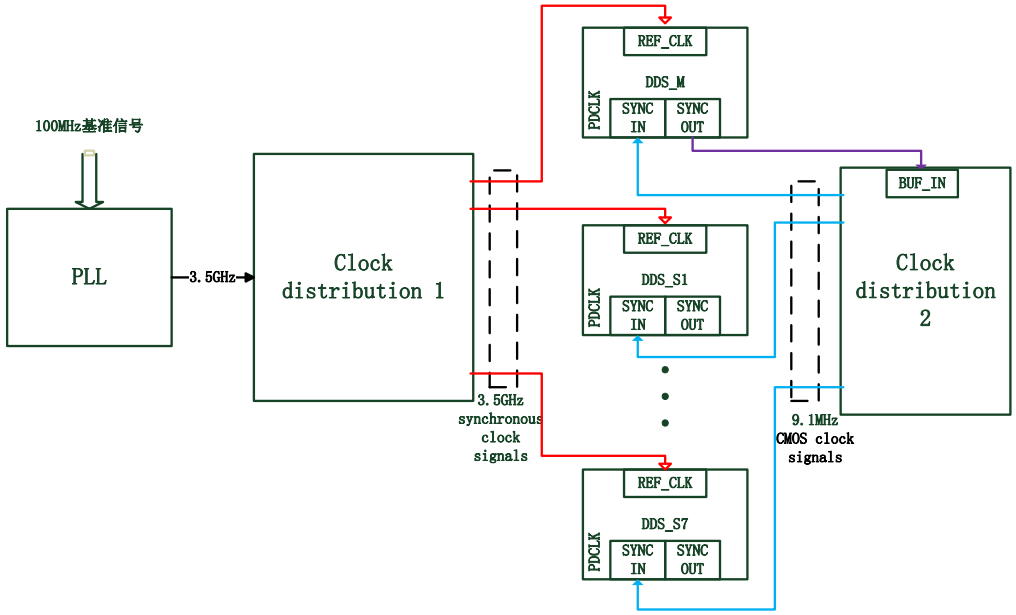

Fig. 3 Design of system clock

4. Conclusion

Base on the study of wideband LFM signal generator method, this paper designs and achieves a multiple channels synchronous wideband LFM signal generation generator system. The system takes advantage of both multiple channels and synchronization. It has complementary performance of the both characteristics. The system meets the needs of the existing signal source of multi-channel synchronous signal generator. The system lay a good foundation for the realization of double wave-band digital array radar.

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