Hardware Implementation of Radio Signals Fast Digital Detection and Demodulation Algorithms

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***Abstract*—We are considering the capabilities and the technical features of the fast digital detection and demodulation algorithms for the signals of various modulation formats as they are realized in programmable logic devices. We show that simultaneous multitype signal processing devices can be implemented in real time.**

Keywords-phase-shift keying; detection; demodulation; digital processing; binary coding; hardware implementation

I. INTRODUCTION

In radio engineering, radio signals with various modulation formats are widely used [1, 2]. One of the main objectives is to develop the full-speed digital algorithms and devices for their detection and demodulation with the minimum set of simple arithmetic operations performed over an input signal period. In papers [3, 4] basic fast digital algorithms of coherent and noncoherent processing of radio signals are introduced. Below we are to demonstrate radio signal detection and demodulation devices that such algorithms make uniformly feasible from the engineering point of view.

II. THE MAIN PART

In paper [3] the basic coherent processing algorithm BA1 of the radio signal $s(t)$ is presented, the block diagram of which is shown in Figure I.

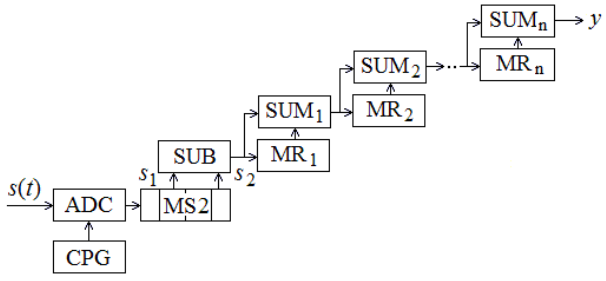

FIGURE I. BLOCK DIAGRAM OF THE BASIC COHERENT RADIO SIGNAL PROCESSING ALGORITHM

For example, at the output of the receiver intermediate-frequency section, the narrow-band radio signal $s(t)$ takes a form of (Figure II)

$$s(t) = S(t)\cos[2\pi f_0 t + \psi(t)] \quad (1)$$

where f_0 is the carrier frequency, $S(t)$ and $\psi(t)$ are the slowly varying amplitude and initial phase. This signal is passed to the analog-to-digital converter (ADC) input, and the quantization points are determined by the signals from the clock pulse generator (CPG) which are synchronous with the received signal.

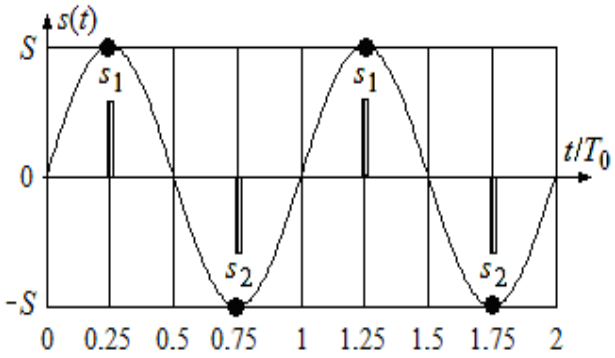

FIGURE II. THE INPUT SIGNAL AND ITS QUANTIZATION IN BA1

ADC forms two samples s_1 and s_2 for each input signal period $T_0 = 1/f_0$ (the case of the quantization in a coherent mode, i.e. at time points consistent with input signal maxima and minima, is shown in Figure II). These samples are stored in the multibit shift register MS2 on two samples. In subtracter SUB the values $s_1 - s_2$ are calculated for each signal period and are accumulated over an information symbol duration being equal to $N = 2^n$ periods. As a result, we get the following value

$$y_{0,i} = \sum_{k=0}^{N-1} \left(s_{1,(i-k)} - s_{2,(i-k)} \right) \qquad (2)$$

where i is the number of the current period, $s_{1,j}$ and $s_{2,j}$ are samples on j-th period.

In order to calculate the sum (1), the fast algorithm (Figure I) is used. It contains $n = \log_2 N$ stages consisting of the summators (SUM_k) and multibit shifters (MR_k), where $k = \overline{1,n}$ is the stage number. Everyone MR_k includes 2^{k-1} cells, in which intermediate results are poked. At the first stage the sum of the two nearest contiguous samples differences is calculated, at the second stage – the sum of four samples differences and so on.

In Figure III the basic algorithm BA2 [4] is shown, with two channels of the quadrature digital signal processing.

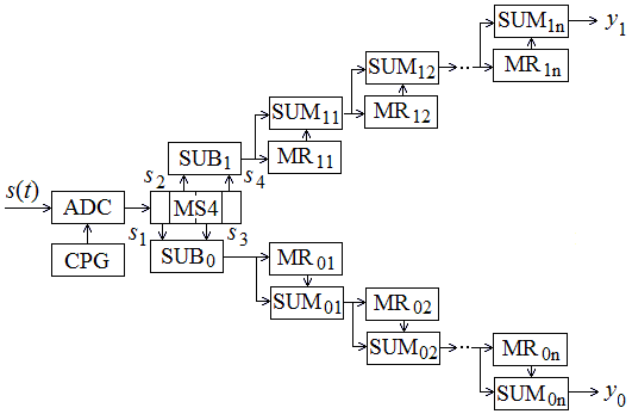

FIGURE III. BLOCK DIAGRAM OF THE BASIC QUADRATURE SIGNAL PROCESSING ALGORITHM

For each input signal period, ADC forms four samples s_1, s_2, s_3, s_4 (see, for example, Figure IV for a coherent mode) which are memorized in the multibit shift register MS4 on four samples.

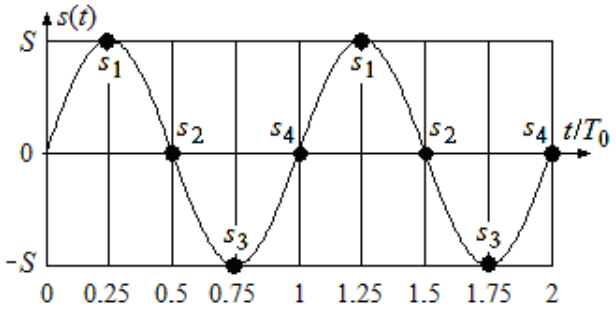

FIGURE IV. INPUT SIGNAL QUANTIZATION IN BA2

In subtracters SUB_0 and SUB_1 the differences of the odd $s_1 - s_3$ and the even $s_2 - s_4$ samples are calculated that are further accumulated over the information symbol duration, as in BA1. As a result, the following responses of the quadrature channels are made

$$y_{0,i} = \sum_{k=0}^{N-1} \left(s_{1,(i-k)} - s_{3,(i-k)} \right) \qquad (3)$$

$$y_{1,i} = \sum_{k=0}^{N-1} \left(s_{2,(i-k)} - s_{4,(i-k)} \right) \qquad (4)$$

The basic algorithms BA1 and BA2 allow us to construct various high-speed digital devices for radio signal detection and demodulation. In particular, in terms of the BA1, we can design the digital coherent demodulator of the binary phase-shift keyed (PSK) signals [2], while in terms of the BA2 the coherent demodulators of the four-position PSK and quadrature-amplitude modulated (QAM) signals [2] can be produced. With the additional transformation in BA2 of the kind of

$$z_i = \sqrt{y_{i,0}^2 + y_{i,1}^2} \qquad (5)$$

We can implement the noncoherent digital radio signal detector [5]. By comparing the adjacent information symbol responses, we obtain the noncoherent digital differential phase-shift keyed (DPSK) signal demodulator [6]. And the two BA2 make it possible to construct the frequency-modulated signal demodulator [7, 8].

In paper [9] the digital noncoherent demodulator of "integrally" coded binary PSK signals is introduced, its block diagram presented in Figure V.

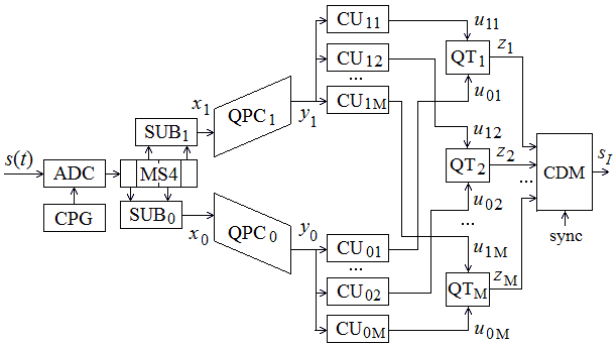

FIGURE V. BLOCK DIAGRAM OF THE DIGITAL NONCOHERENT DEMODULATOR OF "INTEGRALLY" CODED BINARY PHASE-SHIFT KEYED SIGNALS

Block diagrams of the signal quadrature processing channels QPC_0 and QPC_1 are shown in Figure VI. As can be seen, the demodulator support is the BA2 algorithm (Figure III).

The quadrature processing effects $y_{0,i}$ and $y_{1,i}$ are passed to the computing units CU_{0k} and CU_{1k} of the demodulator responses to the kth binary code sequences $a_{i,k} = \pm 1$ (where $i = \overline{1,K}$ is the number of a binary symbol, K is the code length, $k = \overline{1,M}$ is a codeword number, M is the number of codewords). At the CU outputs the following values are formed:

$$u_{0k} = \sum_{i=1}^{N} a_{i,k} y_{0,i} \quad (6)$$

$$u_{1k} = \sum_{i=1}^{N} a_{i,k} y_{1,i} \quad (7)$$

In quadratic converters QC_k the demodulator responses are calculated to the *k*th code combinations

$$z_k = \sqrt{u_{0k}^2 + u_{1k}^2} \quad (8)$$

By the highest of which in the maximum choice device (MCD) the decision is made concerning the received codeword.

It should be noted that in terms of hardware overhead the demodulator of "integrally" coded PSK signals is the most resource-intensive out of all the presented devices.

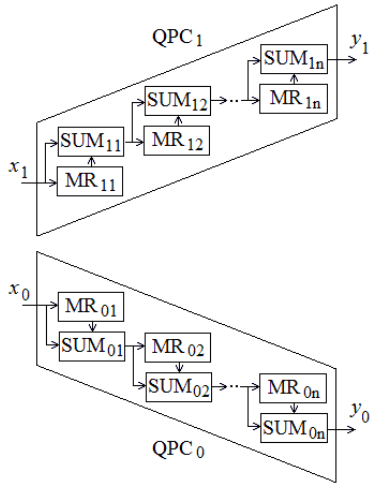

FIGURE VI. BLOCK DIAGRAMS OF THE SIGNAL QUADRATURE PROCESSING CHANNELS

The considered digital signal processing algorithms allow both software and hardware implementation.

Software implementation of the considered algorithms requires a sufficient great number of arithmetic operations consecutively carried out over the input signal period T_0. Such operations also include those referring to the memory address generation in the multibit shifters. Thus, even the use of the high-speed signal processors will already fail to make it possible to process the high-frequency signals, when, for example, $f_0 = 1$ MHz, not to mention that the processor overclocking will lead to the increasing of power consumption of the digital device.

At the same time, hardware implementation of the considered algorithms realized in the programmable logic devices (PLDs) [10] – in Xilinx PLDs, for example – tends to be the most effective one. A broad range of capabilities of various PLD families allows us to choose the most appropriate option according to technical and economic requirements.

The analysis shows that when the ADC capacity is 8 - 10 bits, $N = 64 - 512$ and $f_0 = 10 - 30$ MHz the presented detection and demodulation devices can be implemented using comparatively inexpensive PLDs from the Spartan-6 family (for example, XC6SL25) [11], with the power consumption not exceeding 20-60 mW. In case of the device on-chip mounting, the switching elements (LUT) and triggers (Flip-Flop) are the ones most involved.

In Figure VII as an example the diagram of LUT number is presented demonstrating its percentage in the total number of on-chip while the demodulator of "integrally" coded PSK signals is implemented of the two PSK signals coded by M-sequences with the various PLD types: Spartan-6 (XC6SL25), Kintex-7 (XC7K70T) and Artix-7 (XC7A100T).

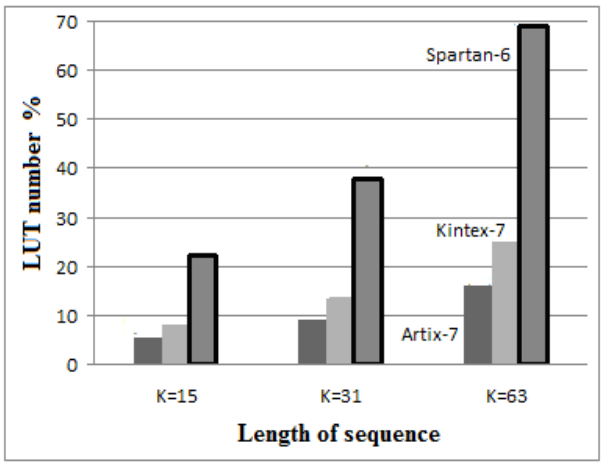

FIGURE VII. NUMBER OF USED SWITCHING ELEMENTS

The similar diagram for the number of triggers is shown in Figure VIII.

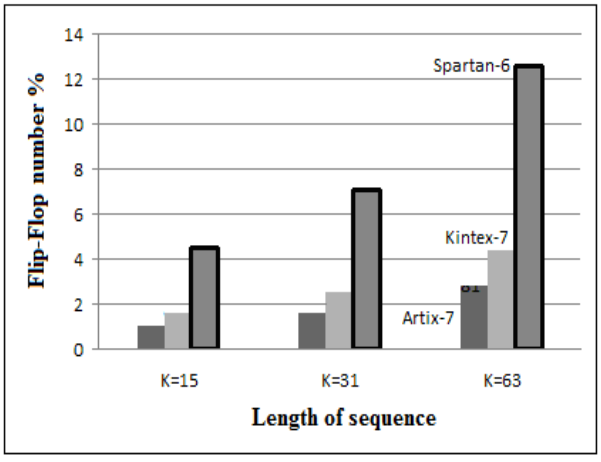

FIGURE VIII. NUMBER OF USED TRIGGERS

The considered coded signals provide high noise immunity, due to the decreasing data transfer rate. The increase in the number of code sequences in their "integrally" processing leads

to the almost proportional increase in hardware overhead. Therefore, the demodulator of "integrally" coded PSK signals based on the Spartan-6 PLD can be applied for the processing of the relatively short codes, for example, a Hamming code (7,4) with $K = 7$ and $M = 2^4 = 16$. When Artix-7 PLD is used, the demodulator of the sufficiently high-power codes can be implemented. In terms of hardware overhead minimization the Walsh codes are the most effective.

In Kintex-7 and, especially, in Artix-7 PLD families lesser hardware resources are used to implement the considered algorithms: in case of the demodulator of the DPSK signals based on the BA2 this value is up to 1 %, and with the demodulator of the two signals "integrally" coded by M-sequences it is up to 5 %. It allows developing many other digital signal processing devices. The top-of-the-line PLDs can process higher frequency signals that are up to $f_0 = 100\text{-}150$ MHz. However, in this case the power consumption increases.

Thus, the possibilities of the modern PLDs including even the mid-range models provide simultaneous implementation of BA1, BA2 and double BA2 (intended for the reception of frequency-modulated signal [7]) algorithms varying by the modes of processing of their $y_{0,i}$ and $y_{1,i}$ responses. Important example is specified in Eq. (2) demonstrating the case of the universal on-chip digital device for detection and demodulation of the various radio signals.

III. Conclusion

The basic fast digital coherent and noncoherent high-frequency radio signal processing algorithms introduced in [3, 4] can be effectively implemented in practice by means of the modern PLDs. Thus, it is possible to construct the specialized and universal digital devices for radio signal detection and demodulation including the demodulation of the "integrally" coded PSK signals.

Acknowledgment

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