A Double Node Upset Tolerant Memory Cell

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Abstract. As we enter the deep submicron era, the steadily shrinking feature sizes make charge sharing much easier among physically adjacent nodes in integrated circuits, which ultimately results in DNU (Double Nodes Upset). In this paper, we propose a 16-transistor memory cell. Hspice simulation shows this cell maintains its original logic status under SNU (Single Node Upset) and DNU, while DICE (Dual Interlock CEll) and Quatro-10T cell may fail. Besides, the 16T cell reduces the circuit area by 33.33%, compared to the other two DNU tolerant cells, Delta DICE and DONUT.

1. Introduction

In the last decades we have witnessed the rapid development of silicon industry. From microscale to nanoscale, the continuous evolution of processing technology has ensured the accuracy of Moore's Law. Diminishing device sizes cause integrated circuits' increasing vulnerability to environment. The applications of semiconductor products in aerospace engineering require chips to be highly tolerant to particle-induced soft errors, especially the upsetting nodes in proximity.

Conventional storage structures, like D flip-flop and SRAM, only have two storage nodes, thus they are highly susceptible to Single Event Upset (SEU) due to charge sharing. By adding two storage nodes, DICE structure enhances its reliability and recovery ability, which makes it generally used in digital circuits, especially in fault tolerant SRAM cells and latches [1]-[5]. But its DNU responses have not been deeply studied yet. Quatro-10T, a neutron radiation robust SRAM cell derived from DICE was provided by [6], however, Quatro-10T's tolerance to SNU and DNU remains to be validated. The so-called "Delta DICE" was proposed by [7], which was said to be resilient to DNU. The main disadvantage is that both Delta DICE and another structure called "DONUT" [8] are composed of 12 inverters, namely 24 transistors. The largely increased area reduces their use in practical products.

In this paper, we mainly present a soft error robust memory cell structure, which consists of 16 transistors and could be used in SRAM cells and latches. Hspice simulation has demonstrated its immunity to SNU and DNU. The paper is organized as follows. Section 2 introduces several soft error hardened structures, including DICE, Quatro-10T and the proposed 16T cell. Section 3 compares the SNU simulation results of the above three cells. Section 4 conducts the simulations of DNU, including DANU (Double Adjacent Nodes Upset), DENU (Double Equivalent Nodes Upset) and other upset patterns. Section 5 draws the conclusion.

2. Structures of Soft Error Tolerant Memory Cells

The structure of DICE is illustrated in Fig.1 (a). N1~N4 and P1~P4 comprise of the main part of the interlocked inverters, while N5~N6 are the read-out circuit. Node A is equivalent to C, while B is equivalent to D. If A stores logic "1", then C should store "1". To the contrary, B and D store "0". Fig.1 (b) is the topologically equivalent structure of Quatro-10T, which is actually a variant of DICE by changing the connections of nodes. The relationship among storage nodes A, B, C and D is the same with that of DICE.

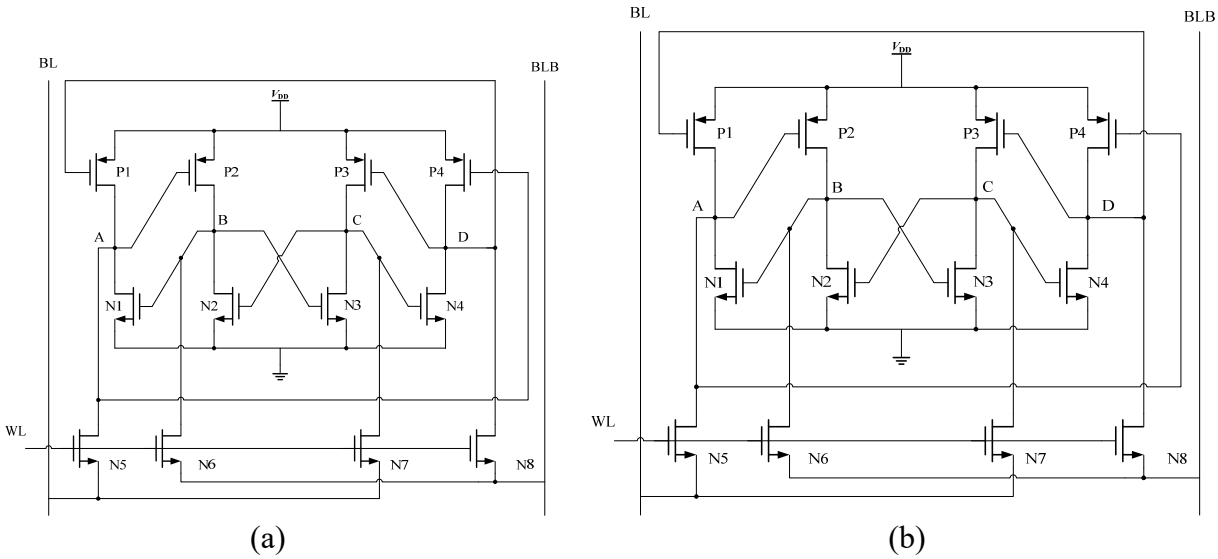


Fig. 1 DICE (a) and Quatro-10T (b)

The proposed 16T DNU immune cell is shown in Fig.2, where the read-out circuit is omitted for simplification. The cell consists of eight NMOS transistors, N1~N8, and eight PMOS transistors, P1~P8. A, C, E and G are equivalent storage nodes, so are B, D, F, H. This means, for example, A, C, E and G are supposed to keep the same potentials. If the stored bit is "1" for A, then C, E and G should be "1"as well. Oppositely, B, D, F and H should store "0". The most important feature of our 16T cell is the transistors that nodes depend on are all spatially separated, like node A depends on the operation modes of two apart transistors P2 and N6, which may enhance its tolerance to DNU.

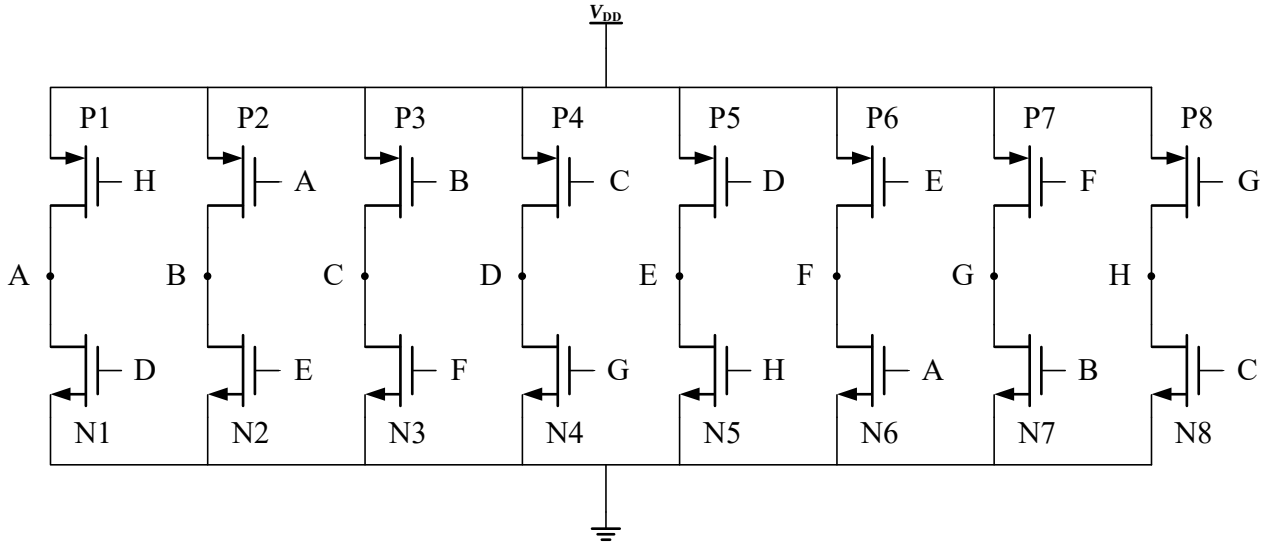


Fig. 2 The proposed 16T cell structure

3. Simulation Results of SNU

In DICE, the interlocked inverters make sure the voltage of one node relys on the voltages of other two nodes. Thus, they can recover to its original logic status even though one node is upsetting. Hspice simulation has shown DICE is resilient to SNU (Single Node Upset).

In the Quatro-10T, B and D control the switch of two NMOS transistors respectively, which could make the logic levels upset if B or D is changing from "0" to "1". Based on TSMC 65nm CMOS device model, all NMOS transistors are set at L=100nm and W=200nm, and all PMOS transistors are set at L=100nm and W=400nm.As we can see in Fig.3, with 1ns width pulse at node B from "0" to "1", the entire logic status of Quatro-10T will upset. The simulation shows that Quatro-10T is not a SNU robust structure.

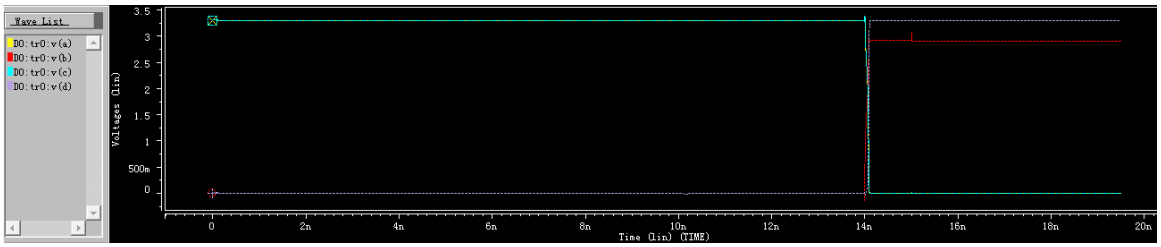


Fig. 3 Quatro-10T's responses to SNU

Table 1 shows the different SNU patterns simulation results of DICE, Quatro-10T and our 16T cell. As for DICE, the gate lengths are designed as 100nm for all transistors. The widths are 200nm for NMOS (N1~N8), and 400nm for PMOS (P1~P4) respectively. Also, we set the same parameters as DICE for the 16T cell.

In the table, A(1-0) mean node A upsets from "1" to "0". "√" means the cell can recover to its original logic status, while "×" denotes electric potentials of these upset patterns fail to recover. For the reason of node equivalence, some simulation results of 16T cell are not listed. Conclusion can be drawn that DICE and the 16T cell are SNU immune structure, while Quatro-10T is not.

Table 1 SNU Simulation Results

Cell\Pattern	A(1-0)	A(0-1)	B(1-0)	B(0-1)	C(1-0)	C(0-1)	D(1-0)	D(0-1)
DICE	√	√	√	√	√	√	√	√
Quatro-10T	√	√	√	×	√	×	√	√
16T	√	√	√	√	√	√	√	√

4. Simulation Results of DNU

Based upon TSMC 65nm CMOS model, we conducted DNU simulation in three aspects, i.e. DANU, DENU and other upset patterns. The device sizes are equal to those in Section 3. We give a voltage rise at node B, and a drop at node C. Fig.5 shows the voltage responses of DICE, two upsetting nodes B and C may cause its failure. Thus DICE is not a DNU robust cell.

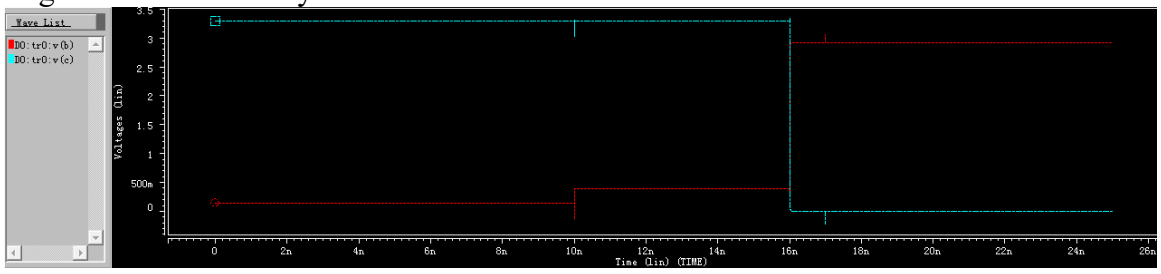
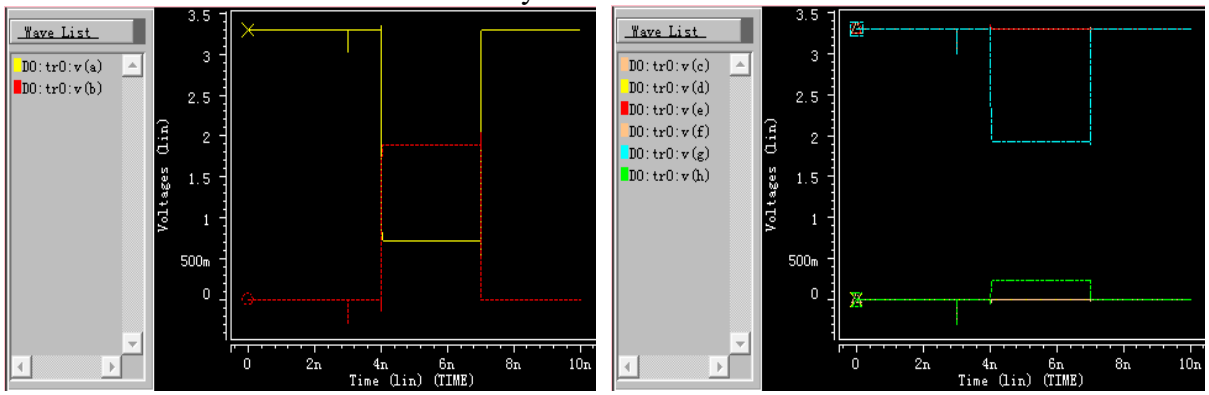


Fig. 5 DICE's responses to DANU

The following figures are the simulation results of our proposed 16T cell. Transient pulses are added to nodes by transimission gates. Fig.6 (a) illustrates the voltage changes at nodes A and B. After the 1ns width pulse, both nodes recover to initial levels. Fig.6 (b) shows that the voltage curves of rest nodes. Most nodes are not affected by the disturbance.



(a) (b)

Fig. 6 The 16T cell's responses to DANU

Table 2 lists the DANU simulation results of DICE, Quatro-10T and 16T cell, where A(1-0)B(0-1) means node A upsets from “1” to “0”, while B upsets from “0” to “1” simultaneously. For the reason of equivalence, some results of 16T cell are not listed. However, 16T cell’s robustness to DANU can be proven by a comprehensive simulation.

Table 2 Double Adjacent Nodes Upsetting Simulation Results

Cell\Pattern	A(1-0)B(0-1)	A(0-1)B(1-0)	B(0-1)C(1-0)	B(1-0)C(0-1)	C(0-1)D(1-0)	C(1-0)D(0-1)
DICE	×	×	×	×	×	×
Quatro-10T	×	×	×	×	×	×
16T	√	√	√	√	√	√

Double equivalent nodes upset simulation results are shown in Fig.7, where we take simultaneous electric potential change from “0” to “1” at nodes A and C as the excitation signals. The volatge waves of A and C indicate the proposed 16T cell is able to recover its initial logic status. Besides DANU and DENU, the cell can tolerate other upset patterns as well, like A(1-0)F(0-1), which is shown in Fig.8. Moreover, the cell is also immune to some triple upset patterns. The DENU simulation results of more nodes are listed in Table 3. In all, the 16T cell is a completely DNU robust structure.

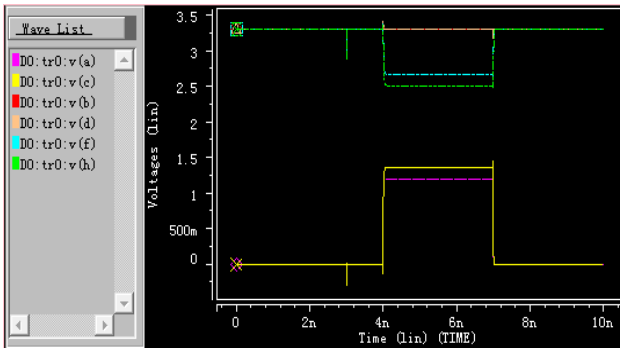


Fig. 7 The 16T cell’s responses to DENU

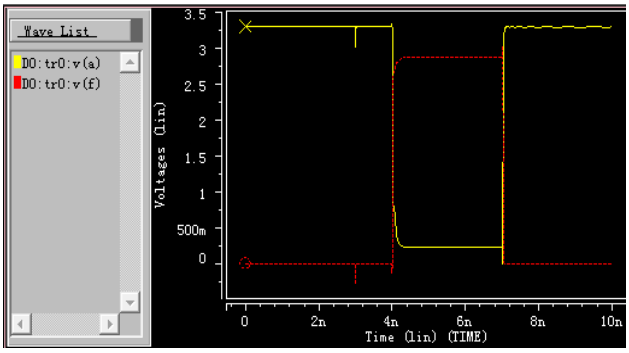


Fig. 8 The 16T cell’s responses to other patterns

Table 3 Double Equivalent Nodes Upsetting Simulation Results

Cell\Pattern	A(1-0)C(1-0)	A(0-1)C(0-1)	A(1-0)E(1-0)	A(0-1)E(0-1)	C(1-0)E(1-0)	C(0-1)E(0-1)
16T	√	√	√	√	√	√
Cell\Pattern	B(1-0)D(1-0)	B(0-1)D(0-1)	B(1-0)F(1-0)	B(1-0)F(1-0)	D(1-0)H(1-0)	D(1-0)H(1-0)
16T	√	√	√	√	√	√

5. Summary

This paper presents a novel soft error robust memory cell, which consists of 16 transistors, not including the read-out circuit. This cell is verified by simulation to be able to tolerate both SNU and DNU, while both DICE and Quatro-10T can’t. Compared to other DNU tolerant structures like Delta DICE and DONUT, our schematic contains less transistors. In summary, the invention can be used as reliable SRAM cells and latches, for its demonstrated DNU immunity, soft error hardness. This 16T circuit structure is being applied for patent.

Acknowledgement

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References

[1]. T. Calin; M. Nicolaidis; R. Velazco. Upset hardened memory design for submicron CMOS technology. IEEE Transactions on Nuclear Science. Vol. 43 (1996), p. 2874-2878

[2]. Qiushi Wang, Lin Jin. A radiation hardened scan flip-flop design with built-in soft error resilience. IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT). Guilin, China. 28 - 31 2014 Oct. p. 1-3.

[3]. Junki Yamaguchi, Jun Furuta, Kazutoshi Kobayashi. A Radiation-Hardened Non-redundant Flip-Flop, Stacked Leveling Critical Charge Flip-Flop in a 65nm Thin BOX FD-SOI Process. IEEE Transactions on Nuclear Science. Vol. 63 (2016), p. 2080-2086.

[4]. Tingting Pang, Wang Kang, Yi Ran. Nonvolatile Radiation Hardened DICE Latch. 2015 15th Non-Volatile Memory Technology Symposium (NVMTS). Tsinghua University, China. 12 - 14 Oct 2015, p. 1-4.

[5]. A. Archana, S Uma Maheswari. Analysis of DICE latch based shift register. 2016 International Conference on Circuit, Power and Computing Technologies (ICCPCT). Thuckalay, Nagercoil, KK Dist, India. 18 – 19, Mar, 2016. p. 1-5.

[6]. Shah M. Jahinuzzaman, David J. Rennie, Manoj Sachdev. A Soft Error Tolerant 10T SRAM Bit-Cell With Differential Read Capability. IEEE Transactions on Nuclear Science. Vol. 56 (2009), p. 3768-3773.

[7]. Nikolaos Eftaxiopoulos, Nicholas Axelos, Georgios Zervakis, Kostas Tsoumanis, Kiamal Pekmestzi. Delta DICE: A Double Node Upset resilient latch. International Midwest Symposium on Circuits and Systems (MWSCAS). Fort Collins, Colorado. 2 - 5 Aug 2015. p. 1-4.

[8]. Nikolaos Eftaxiopoulos, Nicholas Axelos, Kiamal Pekmestzi. DONUT: A Double Node Upset Tolerant Latch. 2015 IEEE Computer Society Annual Symposium on VLSI. p. 509-514.