Research and Design of 16-bit A/D Sample Circuit Based on ADS1146

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Abstract. Analog signal often sampled by A/D conversion in engineering practice, due to external interference and incorrect circuit design, will cause sample accuracy reduce. In order to rejection interference, first a differential input voltage will be magnified by instrumentation, it can rejection noise first, then input amplify signal to TEXAS INSTRUMENTS's ADS1146, it's programmable gain amplifier(PGA) can magnify signal again and internal digital filter can filtering signal again.TL431 can provide precision programmable reference voltage to ADC in order to improve converter accuracy. Finally using software algorithm to reduce interference again. The test result shows that this design method can make sample data stable and improve converter accuracy, it has practical value.

Introduction

In engineering practice, often want to collect some weak analog signal, such as the echo signal of pressure sensor, ultrasonic sensor. These signals are very small, so be amplified, filtering, and then send to A/D conversion chip processing, convert them into digital signals sent to the microprocessor after for display. In the data link, usually exist all kinds of jamming signal, such as the power supply noise and white noise, the device noise, etc. How to effectively suppress noise, usually is the problem that designers have to face. To effectively solve these problems, this paper on the basis of engineering practice, based on years of experience in hardware design, first put forward by using high precision difference instrumentation amplifier simulation of weak signal amplification, because of the difference of two input through subtraction can effectively offset part of the interference, then enlarge input to contain programmable gain amplifier 16-bit A/D sampling chip ADS1146, if the signal magnification is not enough, also can be adjusted by PGA it to 1 to 128 times, the chip embedded digital filter, can effectively remove interference[1-3]. Will finally converted digital signal for high performance microprocessor STM32, again through the software filtering, average filtering algorithm to further reduce interference, will eventually have a very high precision digital signal, and the stability of the display.

Hardware Circuit Design

System Design. The design scheme of the system is shown in Fig. 1, the simulation of small sensor signal through the instrument amplifier INA128 amplifier, and then sent to the 16 bit ADC chip ADS1146 for data acquisition and processing, the digital signal converted by SPI interface and STM32. STM32 collect data for many times, and using the mean filter algorithm for data processing, the results will be processed after the LCD screen display. In Fig. 1, the TL431 provides a reference voltage for the precision A/D acquisition circuit to improve the sampling accuracy.

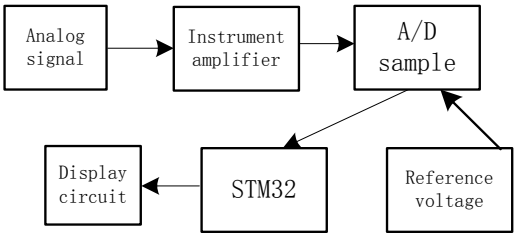

Figure 1. system design chart

STM32F103 Profile. STM32F103 is one of the high performance embedded chips, based on Cortex-M3 technology, which contains many resources, including DMA, RTC, USB, CAN, SPI, IIC interface, etc.. High speed processing of external data can be realized

Instrument Amplifier Circuit Design. The instrument amplifier circuit as shown in Fig. 2, a small analog signal input, using resistance bridge diagram, adjusting the R2 value to produce a voltage difference, through the V1 and V2 input to INA128, Vo as the output voltage. The size of Vo is calculated by formula (1). It can be known that the differential input signal is amplified by 11 times. Appropriate adjustment of the value of Rg, can change the magnification [4-5]. Because it is a differential input, through the V1 and V2 subtraction, can remove the disturbance signal at the two input terminal.

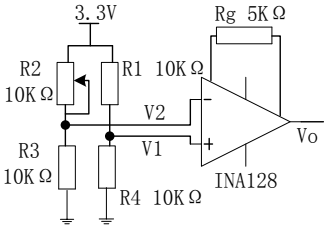

Figure 2. Instrument amplifier circuit

$$V_O = \left(1 + \frac{50K\Omega}{R_g}\right) \times (V_1 - V_2) \tag{1}$$

Introduction to ADS1146 Capture Chip. ADS1146 internal block diagram shown in Fig. 3, you can see from the diagram, AIN0 and AIN1 for 2 - channel analog input terminal, you can do with 1 - channel differential inputs. PGA for a programmable gain amplifier module, Delta Sigma module for AD convert module, provided by REFP and REFN Positive and Negative voltage reference that contains the digital filter Unit, the internal crystal oscillator generates the clock signal, the maximum sampling rate is 2KSPS.SPI Interface provides the signal connected to the microprocessor [6-7]. By SCLK, DIN, DOUT, CS, and so on signal lines connected to the STM32, read the converted 16 - bits digital signal.

Design of the Reference Voltage Circuit. Reference voltage adjustable shunt voltage reference chip tl431, its accuracy is up to 0.5, the design circuit as shown in Fig. 3.Calculation of output reference voltage for example, an equation (2) below. Adjust the resistance of the R1 and R2, you get different output voltage vo.

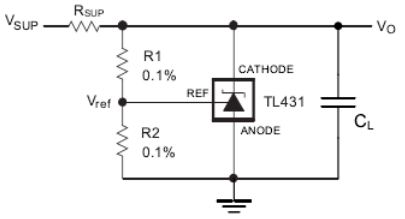

Figure 3. Design of the reference voltage circuit

$$V_O = (1 + \frac{R1}{R2}) \times V_{ref} \tag{2}$$

Software Design and Filtering Algorithm

Software Timing Diagram. In STM32F103 software development, the programming language is C language, the compiler environment for MDK5.0. programming, first initialize the SPI interface, set the sampling rate of ADS1146, PGA amplification, and then according to Fig. 4 to read and write timing of ADS1146 acquisition cycle 100 times, and then remove the bubble sort, sort after the maximum value and the minimum of 15, average with the remaining 70 data, will be sent to the TFT true color display [6-7]**.**

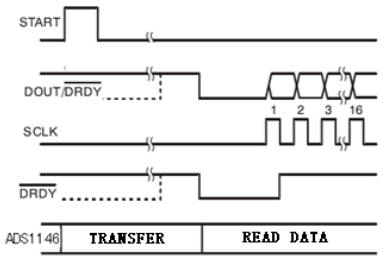

Figure 4. SPI read data of time sequence

Software Filter Processing. In the software filter, the first to bubble sort, bubble sort algorithm is described as follows:

First, from the first element of the array to compare the two adjacent elements, such as the front than the back of the large, exchange, otherwise, to compare the following two adjacent elements; for N elements, the first order finished, will be the largest element to the final; second times when compared with N-1 the rest of the elements or start from the first element of pairwise comparison, second times more, can produce a large number of times; in turn down, for a total of N elements, N-1 Times Ranking, can be completed in ascending order [8].For the 100 cycle of data collected according to the ascending order is completed, because of the presence of interference, the maximum and minimum values must be part of deviate from the actual value, we will remove after the average is more close to the actual value.

Test Results

First we set the internal register ADS1146 SYS0, which the BIT4, BIT5, BIT6 these 3 bits to determine the magnification of PGA. As shown in Fig. 7. When BIT4BIT5BIT6=000, PGA=1; PGA=2; when BIT4BIT5BIT6=001, when BIT4BIT5BIT6=010, PGA=4; PGA=8; when BIT4BIT5BIT6=011, when BIT4BIT5BIT6=100, PGA=16 and so on; when, 111, PGA=128.

By setting the SYS0 register fourth to determine the sampling rate of ADC (SPS), when the fourth is 0000, SPS=5; 0001, SPS=10; 0010, SPS=20; and so on, 1111, SPS=2000.

Set different PGA and SPS, the ADS1146 will have a different effect on the digital filter and the number of A/D conversion. Fig. 5 and Fig. 6 show the corresponding relationship between [9], frequency and gain at different sampling rates. It can be seen from the figure that the digital filter can attenuate the interference signal very well.

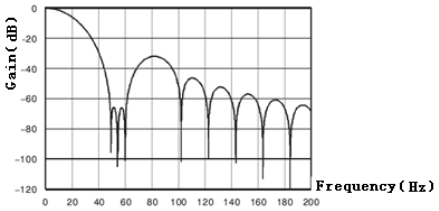

Figure 5. Sampling rate for 100SPS digital filtering effect chart

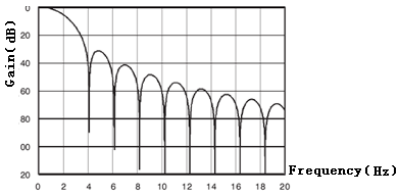

Figure 6. Sampling rate for 1000SPS digital filtering effect chart

As can be seen from Table 1, the noise is effectively suppressed. Table 2 lists the number of valid data bits that are actually obtained after the removal of noise under the same conditions. As can be seen from the table, when the PGA is not large, the sampling rate is not high, basically reached the 16 bit data. It can be seen that the design of noise suppression is relatively good.

Table 1 In VREF=2.048, AVDD=5V, AVSS=0 when the noise size (V)

SPS	PGA=1	PGA=4	PGA=16	PGA=64	PGA=128
5	62.5	15.6	3.91	0.98	0.49
20	62.5	15.6	3.91	0.98	0.55
80	62.5	15.6	3.91	0.98	0.99
320	62.5	17.6	4.3	2.44	2.34
2000	273	67.1	19.2	6.93	6.48

Table 2 Valid data bits in VREF=2.048, AVDD=5V, and AVSS=0

SPS	PGA=1	PGA=4	PGA=16	PGA=64	PGA=128
5	16	16	16	16	16
20	16	16	16	16	15.8
80	16	16	16	15.8	15
320	16	15.8	15.8	14.7	14.1
2000	15.1	14.3	13.5	13.2	12.8

Conclusion

In order to solve the interference in the A/D sampling data link, the hardware circuit design of the hardware circuit is proposed, and the hardware circuit of the device with low noise, high precision and zero drift is selected. In order to improve the number of A/D conversion, the low noise, the 16 bit conversion chip with PGA and digital filter are chosen to simplify the design of hardware circuit, and the ability to resist noise is improved by TI. In the software design using bubble sort algorithm [10]. Through the practical test, the hardware circuit can realize the effective amplification of small signal, and through the software filter processing, can effectively restrain the interference, making the data reliability, stability, accuracy greatly improved. This kind of software and hardware combined with noise suppression method has certain application value.

References

[1] Liu Jun. An example of STM32 [M]. Beijing: Beihang University press, 2012,8. Instruments.

[2] Texas TI high performance analog devices in Colleges and universities application guide [M]. Shanghai, 2014,3

[3] White poetry. The fundamentals of Analog Electronic Technology (Fourth Edition) [M]. Beijing: Higher Education Press, 2009,6

[4] Zhou Qiang, Liu Zhigang, et al. Application of Calman filter in precision machine tool assembly process error state estimation [J], Journal of Xi'an Jiao Tong University, 2015,49 (12): y1-y8.

[5] Gong Zhongliang, Li Yao. The pulse signal acquisition circuit design and optimization of [J] based on photoelectric sensor, electronic devices, 2014, 37 (4): 658-661.

[6] Chen Xiaoyan, Cheng Zhijiang, Jiang Bo, Zhu Yulong. Digital filtering method based on multi-sensor signal fusion [J], electric drive, 2015, 45 (2) 54-57.

[7] Huang Jue, Yan Bing, Chen Haowen. Centralized nonlinear robust filtering algorithm of Calman [J], the research and application of computer, 2015,33 (1) 110-114

[8] Gao Min, Zhang Heng, Xu Chao. An improved strong tracking volume Calman filter for maneuvering target tracking [J], modern defense technology, 2015,43 (6) 155-161

[9] Zhang Zhijian, Zhou Fengxing, Lu Shaowu. [J] high speed data acquisition system based on AD7760 instrument technique and sensor, 2015, (1): 24-26

[10] Yang Bo, Zhang Jiahong, Li Min, Gu Fang. Multi-channel data acquisition system based on [J] ARM, instrument technology and sensor, 2015, (2): 104-107

