# Hardware Design of Online Monitoring Systems for Partial Discharge of High-voltage Cables (Part Two)

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**Keywords:** Hardware Design, Online Monitoring Systems, Partial Discharge of High-voltage Cables **Abstract:** From the aspects of signal conditioning module and data acquisition module, this paper discusses the hardware schematic design of online monitoring and positioning systems for partial discharge of cross-linked polyethylene cables. The correctness and effectiveness of the method disclosed in the paper are proved by field operation of the online monitoring and positioning system for partial discharge of cross-linked polyethylene cables.

### Introduction

Hardware of the online monitoring and positioning system for partial discharge of cross-linked polyethylene cables includes a power management module, control & processing module, signal conditioning module and data acquisition module, etc. <sup>[1-3]</sup> This paper focuses on the design of signal conditioning module and data acquisition module, while the power management module and control & processing module are to be discussed in a separate paper on the same theme.

## Hardware Schematic Design

## **Signal Conditioning Module**

To ensure simultaneous sampling of partial discharge signals and power frequency information of the three phase lines of the cable, four independent analog acquisition channels are designed for the partial discharge signal collector.

Different cable tunnels, test time and test sites have different noise levels <sup>[4,5]</sup>. Therefore, the analog sampling channel is based on two AD8250 programmable amplifiers. Each amplifying channel is composed of four amplification stages, and AD8250 programmable amplifier's adjustable gain range is 1, 2, 5, and 10 (IO control via FPGA). The programmable amplifier's gain table is shown as Table 1.

According to the specific field condition, the amplification factor can be set via software so as to obtain partial discharge signals with the highest-possible sampling precision.

Adjustable gain	First-stage amplification	Secondstage amplification	Third-stage amplification	Differential drive amplification	Total gain	Upper-limit frequency	
1	10	1	1	10	100	17MHz	
2	10	1	2	10	200	15MHz	
3	10	2	2	10	400	15MHz	
4	10	2	5	10	1000	10MHz	
5	10	5	5	10	2500	10MHz	
6	10	5	10	10	5000	7MHz	
7	10	10	10	10	10000	7MHz	

Table 1 Programmable amplifier gain table

The low-pass filtering module is a three-order Butterworth filter. Of all types of passive filters, Butterworth filter has the smoothest pass band <sup>[6]</sup>. The conditioning circuit is shown in Figure 1.



As ADC is a bipolar chip, the signal must go through single-ended to differential conversion before entering ADC, which is illustrated in Figure 2 below.



Figure 2 Single-ended to differential conversion circuit

#### **Data Acquisition Module**

DAU is responsible for field signal acquisition, processing, and transmission. The acquisition system mainly includes an analog acquisition unit, a master control unit and a logic control unit. Its structure is illustrated in Figure 3 below.



**Figure 3 Acquisition system** 

AD9218 is a dual-core 10-bit single-chip analog to digital converter (ADC) for sampling, with an embedded sample-and-hold circuit. It is featured by low cost, low power consumption, small size, easy-to-use and other characteristics [7,8]. Working at a conversion rate of 105 MSPS, it shows excellent dynamic performance throughout the entire operating range. Each of the channels can work independently.

Merely one 3.0V (2.7V -3.6V) single power supply and one clock will be enough for the ADC to work at full capacity. For most application scenarios, there is no need for an external reference voltage source or drive device. The digital output is TTL/CMOS compatible, and a separate output power supply pin supports the 3.3V or 2.5V logic interface.

Clock input is TTL/CMOS compatible, and 10-bit digital output can be powered by a 3V (2.5V-3.6V) power source. User-selectable options offer a combination of power-down modes, digital data formats, and digital data timing schemes. In power-down mode, digital outputs are driven to a high-impedance state. The high-speed AD sampling circuit is shown in Figure 4. Figure 5 is a photo of a real partial discharge signal collector.



Figure 4 High-speed AD sampling circuit



Figure 5 A photo of a real partial discharge signal collector

### Conclusions

Since put into operation, the online monitoring system for partial discharge of high-voltage cables has performed satisfactorily, proving that the said hardware design method is correct and effective.

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