Design of a Power Amplifier using MESFET at 2.7GHz ~ 3.1 GHz

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Abstract. In this paper, a linear power amplifier with MESFET tube is simulated and optimized by the application of ADS software and S parameter method. The MESFET tube is a kind of low distortion power FET provided by the company of Excelics and its tag is EFC480C. After optimizing，the size of the power amplifier proposed is 15mm×20 mm which is rather small among the similar designs. The gain of the amplifier proposed is over 11 dB at the 2.7GHz ~ 3.1GHz, and the output power (sat) of the amplifier is over 30 dBm. The power fluctuation of the amplifier proposed is less than 1 dB, and the input/output in VSWR is less than 2. The performance of the proposed amplifier is outstanding proved by simulation and testing.

Introduction

Using MESFET in the production of microwave hybrid integrated circuit not only makes the volume of the devices smaller than shell packaging devices, but also eliminates the harmful effects of the packaging parameters.

The Class A amplifier has the significant linearity. Static IV curve of the device is usually used to determine the large signal load line impedance (RL), and the class A amplifier is designed with small signal S parameter method [1]. Specific steps are as follows: choose the appropriate MESFET, determine the operating quiescent point and the best output load impedance, design output and input matching circuit network according to the output circuit in the input plane mapping.

Circuit Design and Experiment

Indicators of the Power Amplifier. The indicators of the power amplifier includes: operating frequency ranges from 2.7GHz to 3.1 GHz; gain more than or equal to 11 dB; output power P (sat) more than or equal 30 dBm; power fluctuations less than or equal 1 dB; input and output VSWR less than or equal 2 and the size is 15mm × 20 mm.

Selection of the Tube Core. The first step is to select the right tube core, GaAs chips typically need to to be soldered on the carrier with gold-tin alloy[2,3]. For this, the back of the chips need to be metalized and contacts should be compatible with the thermo-compression bonding process. In reference of the audit objectives, a GaAs FET tube core has been chosen. The tube core is low distortion Power FET EFC480C produced by Excelics, whose gate width is 4.8mm.When the tube core is working in the typical conditions, Vds equals 8V and Ids equals 500 mA. The gain is 18 dB in the frequency of 2GHz. While the power is 1 dB, the compression point presents 32dBm. The source of the core tube without ground connection will need to connect source to ground by gold bonding.

Determine the Static Operating Point and the Load Impedance. Determine the static working point with the work type of amplifier [4]: According to the requirements of linear power amplifier, the

tube bias should be in the CPI. Static drain current Id is about half the saturated drain current Idss, drain bias voltage Vd is 8V and the gate bias Vg is about -1V. Quiescent point can be adjusted according to actual situation.

Determine the load impedance through load line method: the optimal output impedance real part is determined in accordance with the calculated requirements of the tube output load impedance line[5]. The formula for the line load is RL = (Vb-Vs) 2 / (2Pout), wherein Vb is the drain bias voltage and Vs is the knee voltage in V - I curve. For EFC480C Vs equals 2V, the value of Pout can be set 1.5W, finding RL equals 12Ω.

It is noteworthy that to identify bias voltage and maximum output power of GaAs MESFET, the critical parameters is the breakdown voltage. If the load resistance and RF output voltage is too large, it is easy to breakdown. Therefore, it should be determined whether the output voltage will be into the breakdown region. It should meet the standard 2V_b-Vs <BVgd-Vp, wherein BVgd is the gate-drain breakdown voltage, Vp is (gate-source) pinch-off voltage. BVgd of EFC480C is about 20V while Vp is about 2.5V. So the load choice is impedance.

Only when the load impedance between the two ends of the controlled source is a real number, the maximum output power can be got. So the imaginary part of the output load impedance in the matching circuit should resonate with the MESFET drain-source capacitance Cds. During the matching network design, it needs to absorb the imaginary part of the output impedance to make a comprehensive matching network. Cds can be fitted according to the small-signal equivalent circuit parameters and S parameters of the tube. In the light of S parameters provided by Excelics, component values of the MESFET small signal equivalent circuit are fitted through ADS simulation software and small signal circuit is represented as Fig.1:

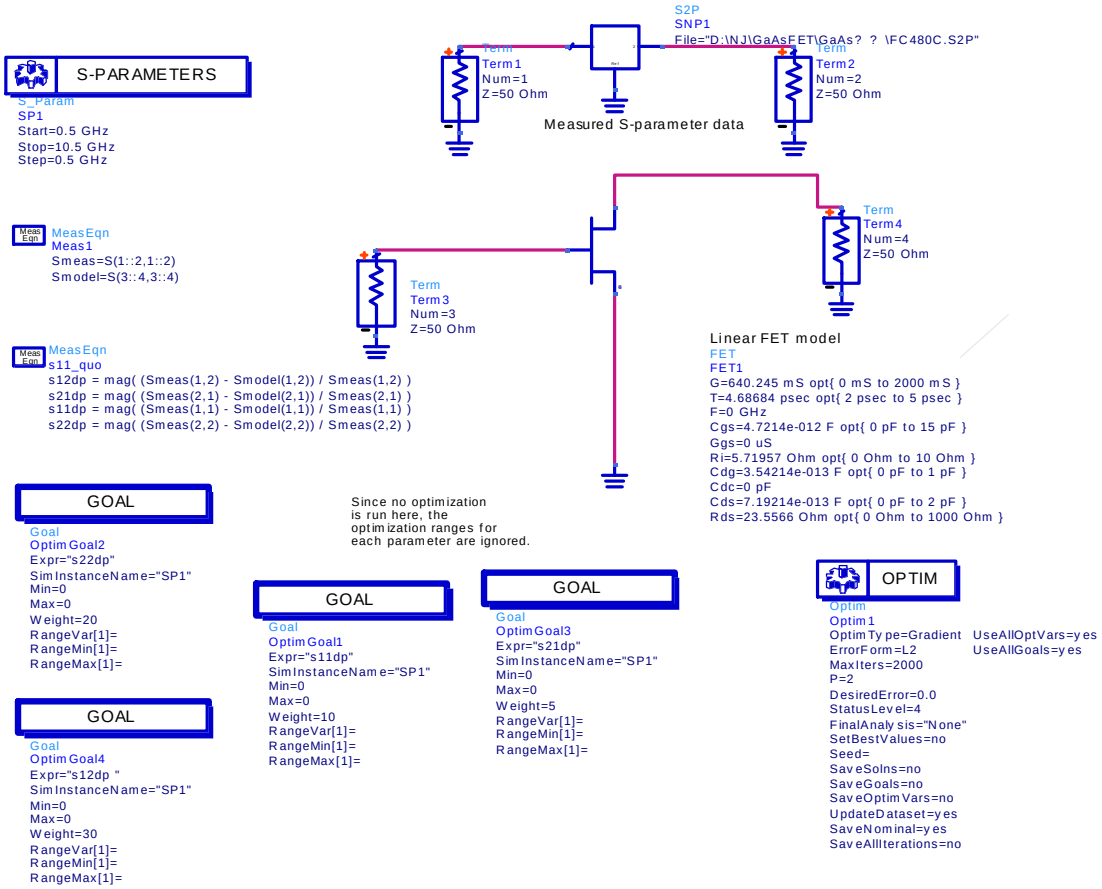

Fig.1 The small signal equivalent circuit

The fitting result indicates that Cds equals 0.72PF. The load admittance resonates with Cds, therefore the load admittance valuation is given as: YL = GL-jwCds wherein GL = 1 / RL = 0.083s. It is available that YL = 0.083-0.014 * j and load impedance ZL = 1 / YL = 11.85 + 2.02 * j.

Estimate output power: Since the load impedance in parallel of the current source is a real number, the AC component and load current of the drain voltage are in phase. The output power can be given as PL = (1/4) (Vb-Vs) Imax = 1.5W.

Circuit Design and Simulation.

A. Bias circuit

Quarter-wavelength band line offers subtle bias while the resonant capacitor is adopted to achieve RF ground in the bias line terminal. The RF signal is isolated by inductance and RF signal and power ripple are filtered by different capacitance.

B. Design output matching circuit

To a large extent, output matching circuit determines the maximum output power and the power efficiency. It requires that output load impedance matching circuit provided the calculated load impedance of the tube core. We use simple and practical L-type low-pass matching circuit to achieve impedance transformation.

In the literature [1], a number of L / S-band amplifiers are mentioned which shows shorting second harmonic (short circuit) enables efficiency increased by 6 percentage points. In the design process, the output matching network needs to make broadband frequency sweep. Integrated using RF terminal quarter-wave length bias line to suppress second harmonic in some degree will maintain a larger second harmonic attenuation in the output circuit and obtain a short-circuit point. What should be noted is that simulation should be included in the drain bonding of gold matching circuit. The appropriate circuit parameters are obtained after optimizing the circuit by ADS. Topology is shown below:

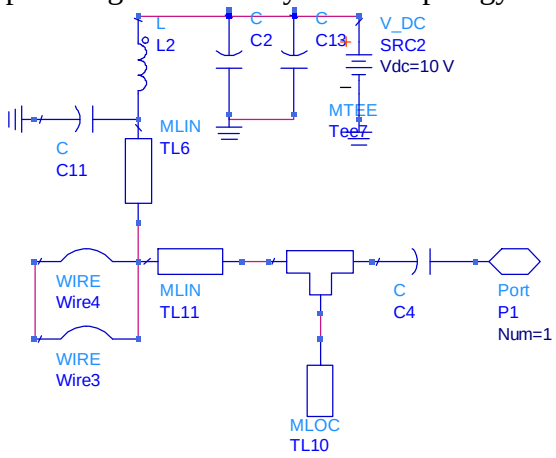

Fig.2 Output matching circuit

C. Design input matching circuit

Input matching circuit design requires providing matching input impedance and ensuring stability, which is a key factor to ensure the design bandwidth. Considering all this factors, a π-type matching circuit is chosen. Specific steps include mapping output circuit to the input plane, designing the input network in the light of conjugate matching method and introducing a shunt resistor to improve the stability. Last but not least, ADS is used to optimize gain, VSWR, bandwidth and stability so that the optimal input matching network can be obtained finally.

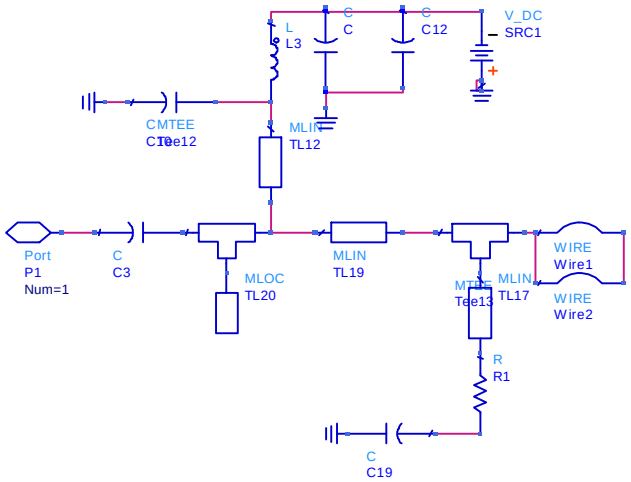

Fig.3 Input matching circuit

D. Simulations with ADS

ADS is used to simulate stability of the circuit which has been shown in Fig 4, k always greater than 1.That means the circuit absolutely stable. ADS S-parameter simulation is shown in Figure 5 which indicates within 2.7GHz to 3.1GHz, the gain is over 14dB and input and output VSWR are both less than 2.

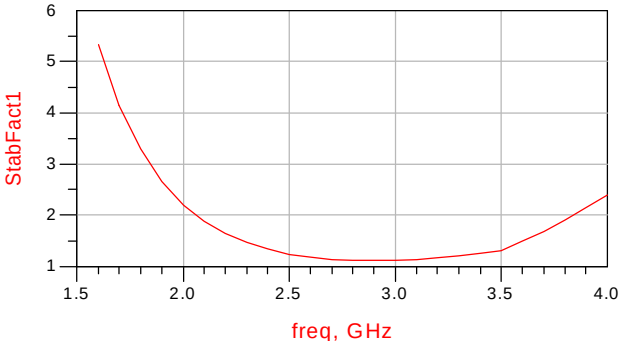

Fig.4 Circuit stability coefficient map

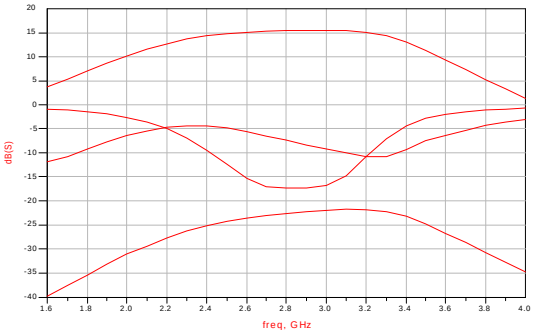

Fig.5 The small signal frequency response

Production, Test and Conclusions

Rogers4003 microstrip plate is selected in the production whose thickness is 0.5mm and permittivity is 3.38. Tube core solders on a molybdenum film carrier whose thermal expansion coefficient is similar to GaAs with gold-tin eutectic. It also should be noted that the carrier chip forms a good combination of alloy type, and otherwise it will affect the performance. Using thermo-compression bonding method, the chip electrode is connected with microstrip by gold bond. What have to be aware of are the parameters consistent with simulation.

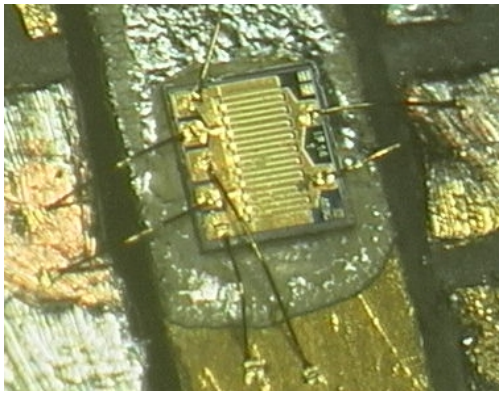

Fig.6 The physical map of the power amplifier

After formed, the circuit is debugged with the copper foil as showed in Figure 6. The results of the final tests show the small-signal frequency response ranges from 2.7 to 3.1GHz, gain is greater than

11dB and input and output VSWR both less than 1.5. The output power is more than 1W, power added efficiency is 23%.The power amplifier performance indicators meets the requirements

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