

Investigation of gate pulse induced interface trap behaviours and its relationship with threshold voltage instability in AlGaN/GaN-On-Si MIS-Hemts

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Abstract. By measuring transfer characteristics before and after a given number of specific pulse cycles applied on the gate electrode for AlGaN/GaN MIS-HEMTs, the threshold voltage (V_{th}) instability is investigated. Furthermore, by measuring the change in transient gate capacitance (ΔC) under different pulses, the effect of applied gate pulse on interface traps in AlGaN/GaN MIS-HEMTs is studied. These gate pulse induced states are believed to be responsible for the V_{th} instability in AlGaN/GaN MIS-HEMTs.

Keywords: Algan/Gan-On-Si MIS-Hemts; trap behaviours; threshold voltage instability.

1 Introduction

AlGaN/GaN MIS-HEMTs, due to its good performance such as high efficiency, high switching speed, and high breakdown voltage, are considered as a promising candidate for next generation power switching circuits [1]. However, the reliability of MIS-HEMTs limits these devices to be commercialized [2]. The main degradation mechanisms such as the current collapse, the permanent increased leakage current, and the instable threshold voltage, are considered to associate with the trapping effect for AlGaN/GaN MIS-HEMTs [2-6]. Deep level Transient Spectroscopy (DLTS) is used to analyse the deep level defects in AlGaN/GaN MIS-HEMTs [7-10]. However, for a DLTS test, a well-controlled temperature cabinet with a wide temperature scope (dozens of K to hundreds of K) is required.

In this work, via changing the gate pulse height or base voltage in the transient capacitance measurement, threshold voltage (V_{th}) instability induced by pulse cycles applied on the gate is studied. Inspired by the mechanism of DLTS, a special transient capacitance measurement is used to study the trap behaviours induced by the gate pulse at room temperature. Based on these measurement results, the interface traps induced by the gate pulses are believed to associate with the V_{th} instability in AlGaN/GaN MIS-HEMTs.

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2 Experiments

2.1 Fabrication of AlGaN/GaN MIS-HEMTs

Fig.1 shows a schematic of the AlGaN/GaN MIS-HEMT fabricated in this work. A 3.8 μm thick unintentionally doped GaN layer followed by a 22 nm $\text{Al}_{0.22}\text{Ga}_{0.78}\text{N}$ barrier are grown on Si substrate using metal-organic chemical vapour deposition (MOCVD). 35 nm SiN_x is deposited as a gate dielectric using low pressure chemical vapour deposition (LPCVD). The gate-drain spacing (L_{GD}) is 10 μm , and the gate-source spacing (L_{GS}) is 2 μm . TiN/Ti/Al/Ti stack is used as Ohmic and Schottky contact in this device. The V_{th} of testing device is about -6.5 V.

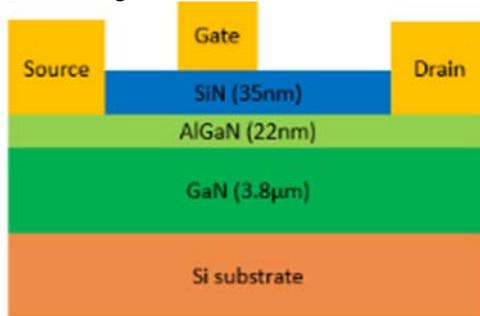


Figure 1. A schematic diagram of the AlGaN/GaN MIS-HEMT fabricated in this work.

2.2 Threshold voltage instability test

Fig.2 depicts the threshold voltage instability test. Specific pulse cycles are applied on the gate electrode, and the drain is connected to the source. The period of the applied pulse cycles is 30 ms, and the pulse width is 5 ms. In this test, all measurements are conducted in the dark environment since light irradiation could affect the trap behaviour.

2.2.1 V_{th} shift and light recovery test

Firstly, a given format of gate pulse stress is applied on the gate for one hour continuously. The base voltage (V_{base}) is 0 V, and peak voltage (V_{peak}) of the pulse is set as 7 V. The change in threshold voltage of MIS-HEMT is monitored by measuring the transfer characteristics. Further, the MIS-HEMT is also illuminated by the lab light to observe the V_{th} recovery.

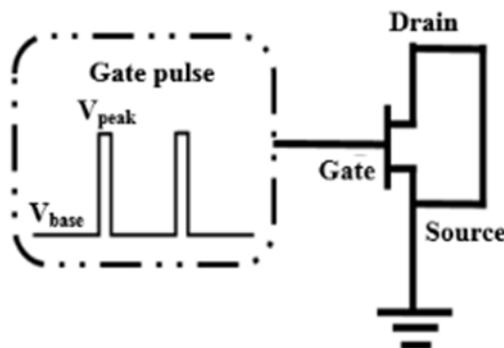


Figure 2. A schematic of the threshold voltage instability test

2.2.2 Impact of pulse height on V_{th} shift

Via changing the height of gate pulse cycles, the impact of pulse height on V_{th} shift is studied. In the first set of this experiment, three pulse cycles with different pulse height are applied on the gate of three MIS-HEMTs for 30 s respectively. These three MIS-HEMTs own the same fresh transfer characteristic. The V_{base} of three pulse cycles is set as 0 V, and the V_{peak} is 3 V, 5 V, and 7 V, respectively. Then after 30 s pulse cycles, the transfer characteristic of three MIS-HEMTs is measured. In the second set of the experiment, three pulse cycles with same pulse height (7 V) but different base voltage are applied to three fresh HEMTs. The V_{base} of three cycles is set as -7 V, -3.5 V, and 0 V, respectively. To maintain the height of three different pulses as 7 V, the V_{peak} is then set as 0 V, 3.5 V, and 7 V, respectively.

2.3 Transient capacitance measurement

In order to evaluate the effect of the base voltage and the peak voltage on the trap behaviours in the MIS-HEMT, a series of ΔC with different input pulses at room temperature is measured. The period and duration of all applied gate pulses are set as 30 ms and 5 ms respectively. Firstly, V_{base} is fixed to -4 V, and V_{peak} is changed from 1 V to 7 V. Then, V_{peak} is fixed to be 3 V, and V_{base} is changed from 1 V to 7 V. A Keithley 590 fast C-V analyser is used to measure the change in transient capacitance. By calculating the capacitance variance (ΔC), a ΔC - t curve can be extracted.

3 Results and discussions

The result of V_{th} shift induced by gate pulse cycles with light irradiation recovery is summarized in Fig.3. With the applying of the gate pulse, V_{th} of the MIS-HEMT is shifted to the positive direction. In addition, V_{th} increases fast at the early stage of the stress, then its variation slows down gradually after 10 min. Light irradiation could significantly recover the V_{th} variation. The result is in agreement with literature [11-13]. Based on these reports, the V_{th} degradation is correlated with interface traps.

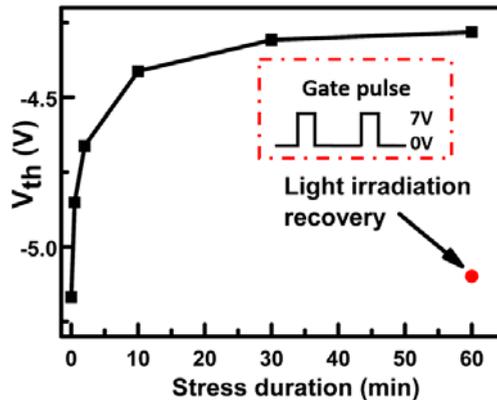


Figure 3. V_{th} variation of the AlGaIn/GaN MIS-HEMT with a continued gate pulse, and its recovery by lab light irradiation.

The impact of pulse height on V_{th} shift is depicted in Fig.4. In Fig.4 (a), with the height of applied pulse increasing, the V_{th} shift is increased. On the other hand, with the same gate pulse height, the V_{th} shift is also dependent on V_{base} as shown in Fig.4 (b): the increase of V_{base} leads to larger V_{th} shift.

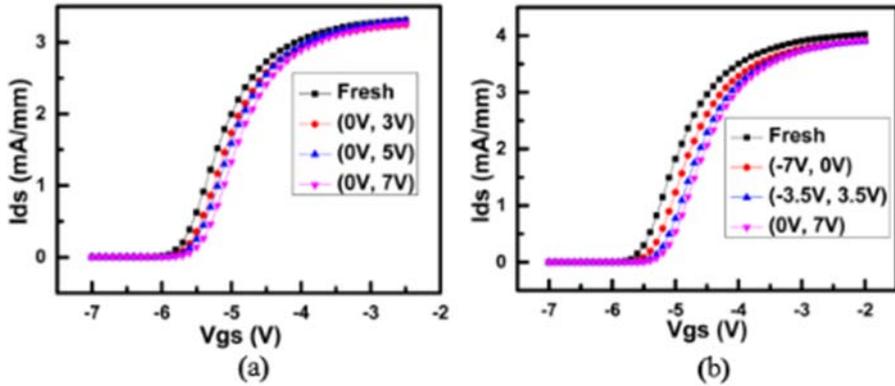


Figure 4. (a) The comparison of transfer characteristics in three MIS-HEMTs under gate pulses with different height (pulse duration is 30s). (b) The comparison of transfer characteristics in testing MIS-HEMTs under gate pulses with different base voltage but same pulse height (pulse duration is 30s).

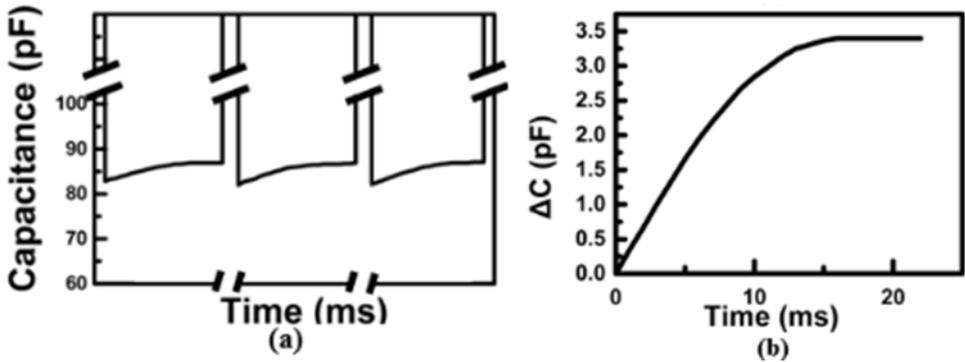


Figure 5. (a) Transient gate capacitance measurement with the pulse applied on the gate in AlGaIn/GaN MIS-HEMTs. (b) The $\Delta C \sim t$ curve extracted from Fig.5 (a).

The change in transient gate capacitance induced by the same gate pulse cycle ($V_{base} = -4$ V, $V_{peak} = 3$ V) for three periods is shown in Fig.5 (a). By calculating the average of capacitance variance (ΔC) of three periods, a $\Delta C \sim t$ curve can be extracted as shown in Fig. 5(b).

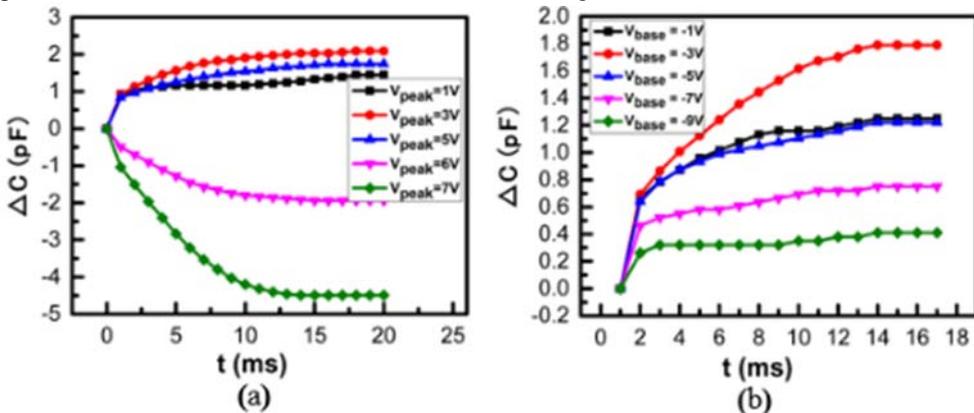


Figure 6. (a) The $\Delta C \sim t$ curves when V_{base} is fixed as -4 V and V_{peak} is changed from 1 V to 7 V. (b) The $\Delta C \sim t$ curves when V_{peak} is fixed as 3 V and V_{base} is changed from -1 V to -9 V.

Via the similar data treatment, the $\Delta C \sim t$ curves under various gate pulses are summarized in Fig.6. In Fig.6 (a), V_{base} is fixed as -4 V, and V_{peak} is changed from 1 V to 7 V. From the figure, it can be

observed that ΔC increases with V_{peak} at beginning and then drops down when V_{peak} is higher than 3 V. It is interesting to note that when V_{peak} is larger than 5 V, ΔC becomes negative and is reduced dramatically. Then, the V_{peak} is fixed as 3 V, and V_{base} is changed from 1 V to 7 V. The corresponding $\Delta C \sim t$ curves are shown in Fig.6 (b). It is observed that with the decrease of V_{base} , ΔC increases firstly and then drops down after $V_{\text{base}} = -3$ V. However, in contrast with the extracted curves shown in Fig.6 (a), the ΔC approaches zero rather than a negative value with further decrease of V_{base} .

It is believed that the trend of ΔC under different conditions can be correlated with the trap behaviours in AlGaIn/GaN HEMTs. When the pulse is relatively small (for example, V_{peak} is set to be only 1 V in Fig.6 (a)), the pulse cannot attract enough free electrons to fill up the deep level traps in the AlGaIn of MIS-HEMT, as in Fig.7 (a). With the pulse height increasing (as well as V_{peak} increases), more free electrons can fill up the traps during the pulse, and thus to be emitted at the steady state, as in Fig.7 (b). Therefore, ΔC starts to increase (e.g. from $V_{\text{peak}} = 1$ V to $V_{\text{peak}} = 3$ V). However, with the further increase of the gate pulse, the pre-existing electron traps in SiN_x bulk layer or at $\text{SiN}_x/\text{AlGaIn}$ interface are believed to be activated, and hence to counter-balance the free electron emission in AlGaIn barrier, as in Fig.7 (c). Thus, the ΔC variation becomes smaller (e.g. $V_{\text{peak}} = 5$ V). To the end, with the gate pulse further increasing (when V_{peak} is set as 6 V or 7 V), the effect becomes more significant, and leads to negative ΔC . By the same token, the negative base voltage is believed to suppress trapping of electron interface traps and cause de-trapping of negative charged states, as in Fig.7 (d). Therefore, ΔC approaches zero rather than a negative value with further decrease of V_{base} .

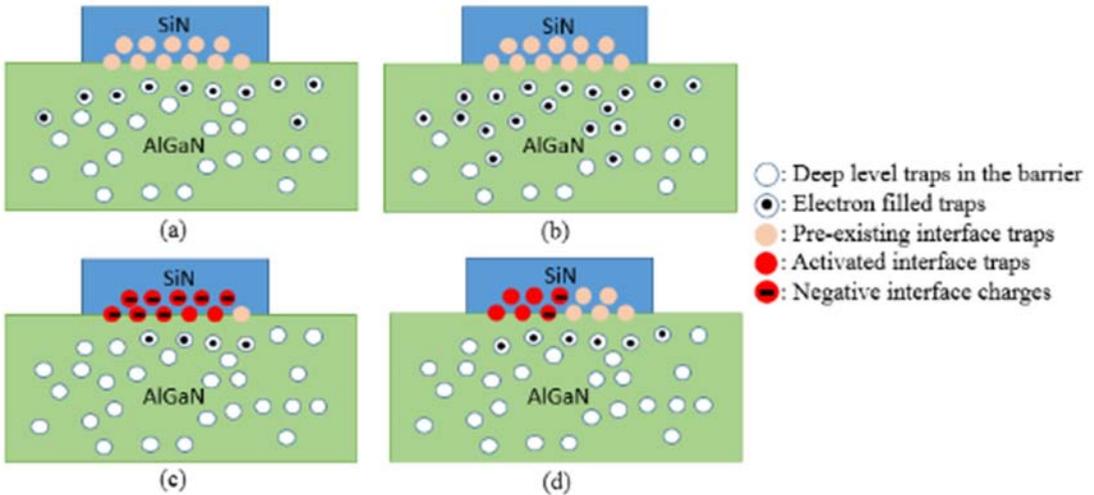


Figure 7. (a) Small pulse cannot attract enough free electrons to fill up the deep level traps. (b) More electrons are attracted to fill up the traps with the pulse height increasing. (c) Further increase of the gate pulse activates the possible pre-existing traps, and induces negative charged states. (d) Negative base voltage suppresses trapping of electron interface traps and cause de-trapping of negative charged states

Based on these observations, the trap behaviours induced by gate pulse are believed to associate with the positive shift of V_{th} in the above experiments. A high gate pulse could induce trapping of electron traps in the SiN_x layer or at $\text{SiN}_x/\text{AlGaIn}$ interface. In addition, the trapping of electron traps induces some negative charged states in the SiN_x later or at $\text{SiN}_x/\text{AlGaIn}$ interface. Because of the negative charged states, the V_{th} of the AlGaIn/GaN MIS-HEMT after the gate pulse stress is shifted to the positive direction, as shown in Fig.3. Since the density of negative charged states approaches to a saturation value after 10 min, the change of V_{th} also slows down and becomes insignificant. In addition, with the height increasing, more negative charged states could be produced, leading to an increase of V_{th} shift as in Fig.4 (a). On the other hand, since negative reverse voltage could suppress the trapping of electrons, the V_{th} shift becomes insignificant with base voltage decreasing, as in Fig.4 (b).

4 Conclusion

In conclusion, the effects of gate pulse on ΔC and its implication on trap behaviours in AlGaIn/GaN MIS-HEMTs are investigated. Furthermore, the relationship of gate pulse induced trap behaviours and threshold voltage instability of MIS-HEMTs is studied.

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