The MAC layer packet transceiver system based on FPGA design and implementation

Mengjiao WU[1, a], JunYANG[1, a, *],CanZHAO[2, b] and Xintao HUANG[3, c]

[1,2,3]School of Information Science and Engineering, Yunnan university, KunMing, China

[a]344786838@qq.com, [a,*]junyang@ynu.edu.cn, [b]781831625@ qq.com, [c]173471638@qq.com

Keywords: MAC protocol layer; FPGA; data packet; throughput rate; gigabit Ethernet

Abstract.Network communication is very important in network transmission.With the continuous improvement of Ethernet technique,the transmission delay of Ethernet MAC(Medium Access Control)will influence communication quality of network.This paper realizes correct send-receive of the Ethernet MAC protocol layer data packet by FPGA,which can reduce transmission delay and enhance throughput rate so that avoid network congestion.It provides technical support of the development of gigabit Ethernet.

INTRODUCTION

Ethernet is a network seems like broadcast which uses CSMA/CD protocol machine-made[1].As a basic media access technology of LAN(Local Area Network),it has lots of advantages,such as high-flexibility,huge medium information content,easily extent and update etc.So Ethernet gets widespread use in enterprise,science and technology ,military and so on.In the way of research and development of Ethernet product,the valuable mask cost of traditional ASIC product is becoming a restraining factor for the development of the integrated circuit.These issues provide a good development opportunity for FPGA.FPGA has short development period and low cost,which becomes the chief choice for the middle and low end of Ethernet product.Therefore,it has a practical significance to realize Ethernet MAC protocol on FPGA and apply it to the related APPs[2].

ETHERNET AND MAC PROTOCOL THEORY

The main functions of Ethernet MAC layer can be divided into many aspects : the construction of a data frame, error checking, transmission control, interface conversion, etc. DIX Ethernet V2 and IEEE802.3 are main forms of Ethernet MAC frame [3]. As shown in figure 1, it shows the Ethernet V2 frame format, the Ethernet frames involves five fields, not only the destination address is 6 bytes long, also the source address. The address which is used to mark the upper protocol type fields has 2 bytes, When repeating the data frames of Ethernet, Ethernet will transmit the received MAC data to a layer of the corresponding agreement automatically.

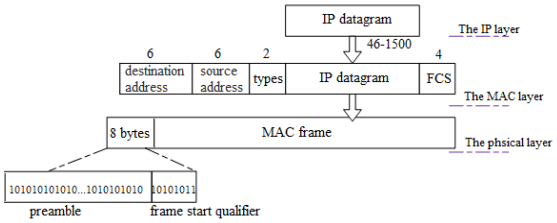

Fig.1 Ethernet MAC frame format

ETHERNET MAC PROTOCOL LAYER PACKET TRANSCEIVER DESIGN

As the key part of Ethernet technology, Ethernet MAC layer protocol is responsible for connecting the physical layer and network layer, at the same time for sending and receiving data packets over the Internet[4].Using the FPGA technology to realize the Ethernet MAC layer protocol in data sending

and receiving process, and apply it to the gigabit network data transmission equipment,the network communication can satisfy realize the demands of high throughput rate transmission.

The overall structure of the Ethernet MAC protocol layer design

In this paper, the design of the Ethernet MAC protocol on the overall function is divided into three modules: data reception, data sending, controlling management[5]. The accomplishment of Ethernet packets encapsulation and unlock bases on data receiving and sending module. Control module is mainly used to communicate with other external PHY chip implementation. The whole design frame can be shown in figure 2 :

Through analyzing the integral design of the system structure, we can give the whole hardware structure of the MAC sub-layer protocol Ethernet block diagram as shown in figure 3, it includes the control module, the module sending and receiving module. In the communication mode selection in the design of the half duplex communication mode, so this network load is low, communication delay is small, the hardware design has simple structure.

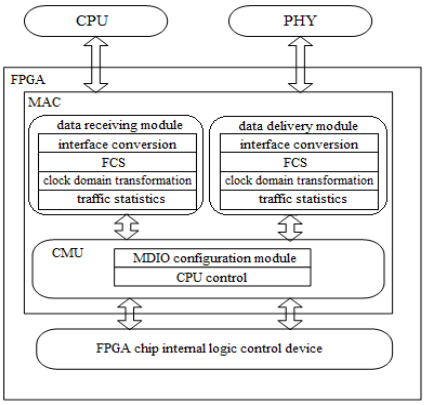

Fig. 2 The overall design frame

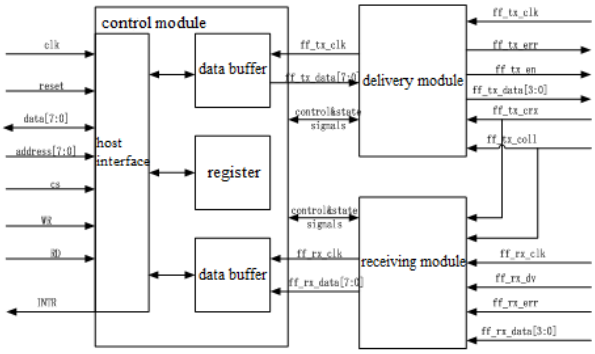

Fig. 3 The hardware structure diagram

The FPGA design of data receiving module

External PHY chip sends the data to the data receiving module, and the related data frames are filled and added after checking and processing, the processed data will be sent to the other internal system logic. Data receiving module in PHY chip interfaces to detect the change of the input signal, according to the input signal for different operation [6].

a) When the input signal is invalid data frame, the module will not make any processing and discard the data frame.

b) When the input signal is effective data frame, the module will receive the input packets, and check the received data, and scanning packets at the same time, then determine whether a packet is populated, if filled, then remove the padding bytes, or do nothing.

At the same time,when module is receiving data packets, three speeds Ethernet IP core will call related module to calculate packet FCS (frame test sequence), stop counting until scan the end of the packet, if the calculated result is zero, that is to say ,the transmission of data packets are correct .According to the process of data processing, the module can be divided into five modules as shown in figure 4: data conversion module, MAC clock domain GMII interface to the system clock domain transformation module, FCS calibration module, cut the filled bytes which is a redundant module, receiving traffic statistics module.

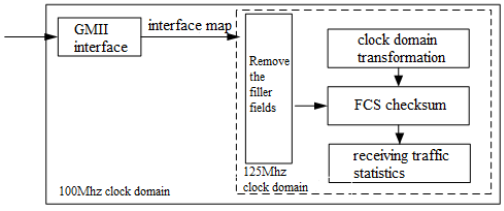

Fig. 4 Data receiving module

The FPGA design of data sending module

Data sending module packs data from the internal interface, then sends packets to the external PHY chip, data sending module is a design of the package for sending, when the system module is ready to send a packet, the module of packet encapsulation are performed. Basing on the Ethernet MAC protocol, packet needs to be sent to the external physical PHY chip in valid data before adding MAC lead frame. And at the same time, in accordance with the CRC - 32 data validation algorithm to detect packet frames used FCS, finally check whether the effective data that is going to be sent goes beyond the effective length of Ethernet data frame, if the valid data is less than 60 bytes, then fill the need for zero byte, finally complete the whole sending process of packets [7]. In essence, the data transmission is an inverse process data reception,and it can be divided into two steps as follow:

a) Conveying the data packets to three speeds Ethernet IP core through the FIFO .ff_tx_data stands for data transmission of the data bus, ff_tx_clk stands for clock,and it can transmit a data in each cycle.The width of the selected data in this paper is 8 bits. that is to say,it is a byte. Ff_tx_sop and ff_tx_eop is a beginning of the transmission packet and a signal of ending. It shows that the data in ff-tx-uflow、ff-tx-full、ff-tx-emty is effective, if ff-tx-wren is 1,it means the writing data is effective. Besides the several main pins , ff_tx_err, ff_tx_rdy, ff_tx_crc_fwd, ff_tx_uflow, ff_tx_full, ff_tx_empty etc, mainly used as a sign to show the state and the emergence of anomalies. Apparently, the meaning s of naming their functions and pins are the same.

b) Conveying the data packets,which are in the IP core of three speeds Ethernet through the external interface (here used GMII) . The gm_tx_d is a data bus of the interface of GMII that can send data , the fixed width is 8 bits. Gm_tx_en is 1 means the data in gm_tx_d is effective, and the physical layer can receive it. Gm_tx_err is 1 means that it will tell the physical layer that the sent data packets are ineffective.

SYSTEM SIMULATION TEST

In this article the Ethernet MAC protocol design implementation scheme uses the FPGA chip of Altera corporation CycloneII, by simulating and testing, it can achieve the basic function of Ethernet MAC protocol layer data transceiver. Additionally, QuartusII is a choice of system simulation testing platform, it found an IP core of the Ethernet, which has three speeds by using QuartusII. In the whole network layer, the IP core belongs to the data link layer, the main task is to send the needed data with head and then send it out after being checked .then receive the physical lines of data packets, finally, send the divided data to users.

Sending packets to test

According to the design of the system structure, sending packets are divided into two steps to complete. Figure 5 is a simulation diagram that can send data.

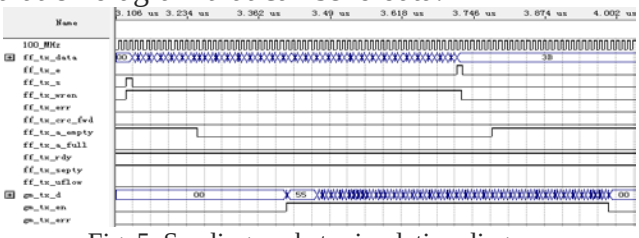

Fig. 5 Sending packets simulation diagram

It can be seen in the figure that the user input data into FIFO, in ff_tx_s and ff_tx_e ,it will come into being a pulse at beginning and ending. and ff_tx_wren is always 1 in the process of writing, other signals are normal. When the user data is half, gm_tx_en is set to be 1, said the data on the GMII interface effectively, and start sending valid data will guide the whole gm_tx_d packets sent.

Receiving packet to test

Receiving packets are divided into two steps. Figure 6 is a whole simulation that shows receiving

data.

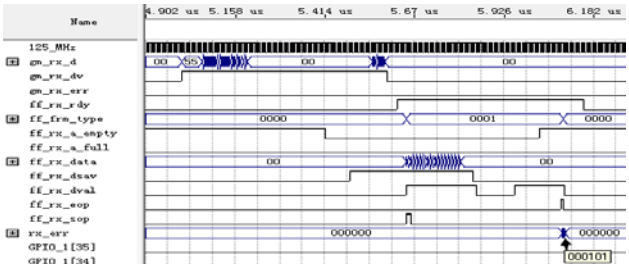

Fig. 6 Packet received simulation diagram

Two steps in this picture can be described as: first the GMII receiveing packets, including 8 bytes of heads and CRC check code that has 4 bytes, then the FIFO send data to the user. In the process of FIFO data transfer, ff_rx_sop and ff_rx_eop produce a pulse in the beginning and ending of data packets, In the process of testing, the length of receiving packets is 0x0014, that is to say it has 20 bytes long, but the smallest length of the data link layer packets is 60 bytes, so it must be padded with zero, it will end when ff_rx_eop shows its length is 60 bytes.

CONCLUSION

This paper analyzes the Ethernet MAC protocol , hardware MAC protocol implementation structure is divided into data reception, data transmission and control management of three modules , mainly for Ethernet MAC packet send and receive in-depth analysis, and using FPGA technology to achieve a data packet send and receive , in addition to control management part using 10/100/100 IP core logic control , and provide the appropriate external interface , including reading traffic statistics , the external PHY chip configuration. After elaborated transceiver module design and implementation , building simulation test platform gives transceiver system-level simulation results. Simulation results show that : FPGA-based platform designed to send and receive Ethernet MAC layer packets fast occupancy rate system to meet real-time communication environment system throughput requirements.

REFERENCES

[1] Zhang Xuekun. Based on the FPGA Ethernet MAC data processing [D]. Chengdu university of technology, 2012.
[2] Gong Feng. The design and implementation of gigabit Ethernet controller based on FPGA [D]. Xi 'an university of electronic science and technology, 2014.
[3] Hou Yi close, Zhang Dong winter, Ding Lei. Based on the FPGA, MAC and PHY gigabit Ethernet digital system design [J]. Science, technology and engineering, 2014, 12:275-279.
[4] Cao Yunpeng. Ethernet MAC layer protocol research and FPGA implementation [D]. Suzhou university, 2011.
[5] Mr. Zhang, Luo Feng. High-speed data transmission system based on gigabit Ethernet design [J]. Journal of electronic science and technology, 2011,01:44-46.
[6] QuXin, yun-feng wu, Li Huadong Zheng Tiance, Dai Lei, Xia Tao. Of gigabit Ethernet data transmission based on the FPGA design and implementation of [J]. Journal of electronics, 2014, 662:662-664.
[7] ChanJie Wu Jie, liu feng. Reliable high-speed data transmission method based on Ethernet PHY implementation [J]. Micro computer and application, 2013:38-40 + 43.