Switching performance of GaN FETs in terms of turn-off resistance characteristics: an experimental study

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Abstract. This study evaluated the AC parasitic capacitances and turn-off resistance of GaN FETs. Moreover, the study proposes an easily adjustable gate drive circuit appropriate for driving E-mode, cascode, and D-mode GaN FETs in the same driver topology. The proposed gate drive circuit involving only positive supply was established to provide not only a positive gate drive voltage to E-mode and cascode GaN FETs, but also a negative gate drive voltage to D-mode GaN FETs. This study also presents a simple circuit for shifting gate drive voltage levels to meet the driving voltage required for fully turning on or turning off GaN FETs. In cascode GaN FETs, the gate drive circuit incorporates additional resistor–capacitor–Zener diode (RCD) circuits applied to achieve a faster discharge rate, thereby increasing the switching speed by offering a negative turn-off voltage when the transistor is engaging in a turn-off process. In D-mode GaN FETs, the additional RCD circuits increase the drain current to enable the gate drive voltage to increase, resulting in the power transistor being turned on, thereby achieving a full conduction state to reduce on-state resistance. This paper presents comparisons of the switching performance of the different GaN FETs through the proposed gate drive circuit.

Introduction

As silicon approaches its performance limits, wide-bandgap semiconductors achieve higher levels of performance, and therefore can replace silicon MOSFETs as next-generation power transistors. Such properties as high electron mobility, saturation velocity, and breakdown voltages render III-nitrides feasible for high-power, high-temperature, and high-frequency applications. Many previous studies have reported that utilizing GaN-based devices offers high-quality performance in power converter applications. Although GaN transistors perform at higher levels than silicon transistors do, the safety-related drawbacks of normally on operation, unique device problems, and lack of proper gate drive circuits have thus far kept them from the market. Present technical issues include E-mode structures, cascode/chip packaging, current collapse, dynamic R_{on} measurement, stray inductance, thermal issues, $R_{DS(off)}$ uniformity sorting, and gate drive design [1]. The current collapse phenomenon affects the voltage rating in the circuit application. Inducing higher levels of performance and designing proper gate drive circuits for meeting the unique requirements and different operating modes of various GaN FETs are both critical issues worth analyzing. For new GaN devices, subjecting them to electrical characterization and implementing suitable gate drivers are necessary. Many GaN FET manufacturers, such as EPC, Transphorm, GaN Systems, and Panasonic, provide guidelines for designing gate drivers. Nonisolated high-side gate drivers use a simple bootstrap with a diode and a capacitor, and an isolated high-side gate with floating isolated power is also a frequently used method of generating gate voltage for high-side drivers. The bootstrap method may not be able to provide accurate gate voltage regulation for GaN FETs, and a bootstrap capacitor clamp circuit is required to keep the high-side bootstrap voltage from exceeding the $V_{GS,max}$ maximum rating. Alternatively, a floating isolated gate drive can be adopted for high-side gate drivers [2].

This study proposes an easily adjustable drive circuit appropriate for D-mode, cascode, and E-mode GaN FETs in the same driver topology. The remainder of this paper is organized as follows: First, the characteristics of laboratory-fabricated GaN FETs are presented; second, the proposed resistor–capacitor–Zener diode (RCD) driving topology and its mechanism are discussed; and finally, a drive circuit developed for evaluating dynamic switching performance is presented.

Characteristics of Fabricated GaN FETs

Studies have demonstrated the characteristics of laboratory-fabricated D-mode and cascode GaN FETs [3-4]. Because of the differences in device fabrication, wire bonding, and packaging, device characteristics must be measured to obtain detailed nonuniformity device information. Figure 1 displays the D-mode and cascode structures of the GaN FETs used in the experiments of this study. All GaN FETs are based on the same 80-mm bare die with different configurations, packaged with TO-3P packaging as an individual D-mode type, or TO-257 packaging as a cascode type. Commercial cascode and E-mode GaN FETs were employed to compare the electrical properties of the devices. The current study analyzed the output characteristics, transfer characteristics, and parasitic capacitances of GaN FETs. Furthermore, this study determined the relationship between device parasitic capacitance and turn-off resistance, $R_{DS(off)}$, to induce a higher level of performance in the circuit application.
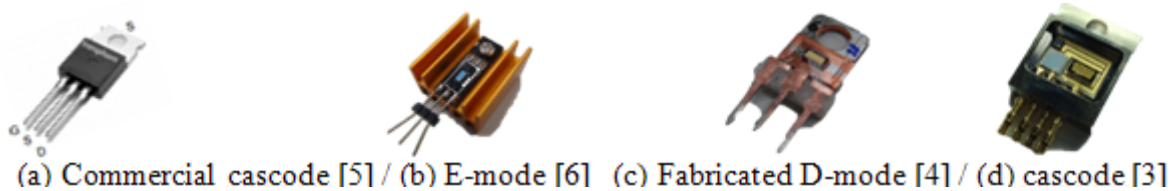

(a) Commercial cascode [5] / (b) E-mode [6] (c) Fabricated D-mode [4] / (d) cascode [3]

Fig. 1. GaN FET devices.

Output Characteristics (I_D-V_{DS})

Figure 2 shows the output characteristics of D-mode and cascode GaN FETs. A test pulse width of 300 μs, pulse period of 300 ms, and duty cycle of 0.1% were applied to measure the I_D–V_{DS} curve characteristics of the devices. In a D-mode device with gate biasing, V_{GS} starts from −5 to 0 V. When V_{GS} = −3 V, the drain current was almost zero; when V_{GS} = 0 V, the transistor was fully on, and the maximum drain current was 25.5 A when V_{DS} = 7 V. By contrast, in a cascode device with gate biasing, V_{GS} starts from 0 to 10 V. When V_{GS} = 3 V, the drain current was almost zero; when V_{GS} = 10 V, the transistor was fully on, and the drain current was in excess of 25.6 A when V_{DS} = 8.5 V. The subplot shows the static on-resistance, $R_{DS(ON)}$, versus V_{DS} derived from the I_D–V_{DS} curve, with $R_{DS(ON)}$ obtained by dividing V_{DS} by I_D. When V_{GS} = 0 V and V_{DS} = 1.5 V, $R_{DS(ON)}$ was 0.16 Ω, whereas when V_{GS} = 10 V and V_{DS} = 1.5 V, $R_{DS(ON)}$ was 0.23 Ω. Because a MOSFET is connected in series with GaN in a cascode configuration, the on-resistance and wire bonding resistance of the connected MOSFET are approximately 0.07 Ω. The recommended gate driving voltages are from -5 to 0 V for D-mode GaN FETs and from 0 to 10 V for cascode GaN FETs.

Transfer Characteristics (I_D–V_G)

Figure 3 shows D-mode GaN FET transfer characteristics (I_D−V_{GS}) for V_{GS} values ranging from −6 to 1 V in 0.1-V increments and a V_{DS} value of 5 V, as well as cascode GaN FET transfer characteristics for V_{GS} values ranging from 0 to 10 V in 0.1-V increments and a V_{DS} value of 10 V. The blue and green lines represent the plots for I_{DS} versus V_{GS} and I_{DS} versus g_m, respectively. The tangent of the resulting curve was derived at the maximum g_m point. The threshold voltage was determined by the intersection between this tangent and the horizontal axis. The threshold voltage of the D-mode device was −2.5 V, whereas that of the cascode device was 4 V; the threshold voltage shifted from negative to positive values. A higher threshold voltage prevents devices from incurring

fault-induced turn-on problems; moreover, a positive threshold voltage is compatible with existing commercial gate drive circuits.
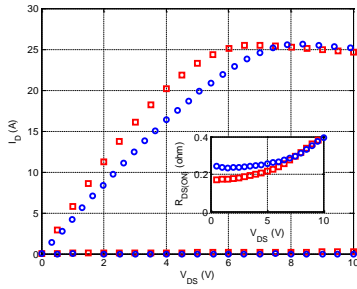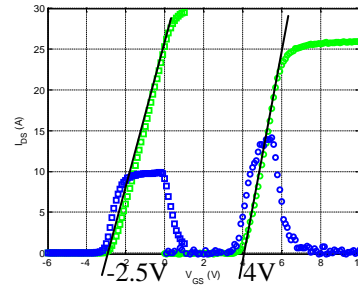

Fig. 2. Output characteristic.

Fig. 3. Transfer characteristic.

(rectangle: D-mode; circle: cascode)

Parasitic Capacitances

Figure 4 shows the parasitic capacitances of the fabricated D-mode and cascode GaN FETs. The measurement was conducted within an AC frequency range of 100 kHz–1 MHz. C_{GS} was measured at 100 kHz, whereas C_{DS} and C_{GD} were measured at 1 MHz, with the oscillation level being 30 mV. In the D-mode GaN FET, the input capacitance C_{iss}, output capacitance C_{oss}, and reverse transfer capacitance C_{rss} values at a V_{GS} of −5 V and V_{DS} of 100 V were 56, 50.6, and 8.64 pF, respectively, whereas in the cascode GaN FET, these capacitance values at a V_{GS} of 0 V and V_{DS} of 100 V were 4350, 110, 1.84 pF, respectively. The parasitic capacitances of the cascode GaN FET are higher than those of the D-mode GaN FET because of the parasitic capacitance of the cascode LV MOSFET.
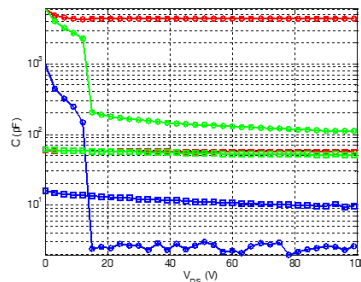

Fig. 4. Fabricated GaN FETs: measured parasitic capacitance (rectangle: D-mode; circle: cascode)

Relationship Between Parasitic Capacitances and $R_{DS(off)}$ for GaN FETs
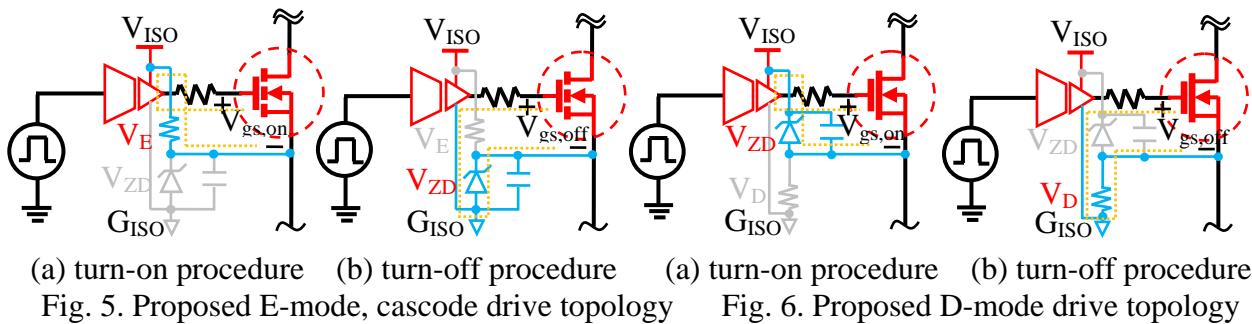
Based on the extracted characteristics of the GaN FETs and the uniformity sorting methods [4], the current investigation further established the relationship between turn-off resistance and parasitic capacitances. The drop in capacitance as V_{DS} increased was engendered by the depletion of free electrons in GaN. Increasing V_{DS} enlarged the depletion region, depleting the inherent 2DEG and reducing its capacitive component. Through previous research, device uniformity can be indirectly screened through turn-off resistance. An isolated gate drive detection circuit was used for screening the devices. An A 1 × (1 MΩ) probe was used to measure (R_L = 1 MΩ), and the power supply voltage, $V_{DD,}$ was set to 24 V. To turn on the commercial cascode [5] , E-mode [6] and fabricated cascode GaN FETs [3], the gate driving voltage was set to V_{GS} = 5 V, and the gate-to-ground voltage was +29 V. When V_{GS} = 0 V, the cascode and E-mode GaN FETs turned off. When Kirchhoff circuit laws were applied, the power supply voltage V_{DD} through $R_{DS(off)}$ and R_L generated the leakage drain current, I_{DSS}. Subsequently, the gate-to-ground voltage waveforms of the fabricated D-mode GaN FET were measured. When V_{GS} was 0 V, the D-mode GaN FET was drained and the source conducted and shorted. The source terminal voltage was +24 V. Because V_{GS} = 0 V, the gate terminal voltage was +24 V; when V_{GS} = −5 V, the GaN FET was off.

Proposed RCD Gate Drive Operation

The method of gate voltage clamping was proposed in [7], and this scheme entails placing a Zener diode and capacitor between the gate and the source for producing negative $V_{GS(OFF)}$. An RCD level shifter using two capacitors, two resistors, and one diode was proposed for generating various negative gate voltages to meet different gate driving levels; the shifting level is independent of the duty cycle.

Referring to the aforementioned studies, the current study proposes RCD gate drive architecture, as illustrated in Figure 5 - 6. Compared with the conventional isolated gate drive circuit, the proposed architecture incorporates an additional resistor, capacitor, and Zener diode in parallel with the input supply voltage of the isolated gate drive amplifier. The various arrangements of the resistor, capacitor, and Zener diode components can provide adaptive gate voltage levels for driving E-mode and D-mode GaN FETs. Placing the Zener diode and ceramic capacitor in parallel with the input isolated supply voltage not only provides gate protection, but also clamps the gate driving voltage within the absolute maximum rating.

For driving the E-mode and cascode GaN FETs, a series resistor, R_S, and a parallel connection of a capacitor, C, and a Zener diode, Z_D, are connected between the terminals of the input supply voltage of the isolated gate drive amplifier: V_{ISO} and G_{ISO}. One side of the series resistor R_S is connected to the positive terminal of the input supply voltage, V_{ISO}, whereas the other side is connected to the parallel connection of the positive terminal of the capacitor C and the cathode terminal of the Zener diode Z_D. The parallel connection of the negative terminal of the capacitor C and the anode terminal of the Zener diode Z_D are connected to the negative terminal of the input supply voltage, G_{ISO}. The source of GaN is subsequently connected in the middle of the series resistor R_S, and the parallel connection of the capacitor C and Zener diode Z_D, as shown in Figure 5. The operating procedure is outlined as follows: When the switch is turned on to provide the power supply voltage V_{DD}, the Zener diode Z_D clamps a voltage, namely V_{ZD}. Simultaneously, the gate terminal with respect to the floating ground G_{ISO} is calculated by $+V_{ISO} - V_{ZD}$. When the switch is turned off, the gate terminal with respect to the floating ground G_{ISO} is the voltage that the Zener diode Z_D clamps, namely $-V_{ZD}$.

(a) turn-on procedure   (b) turn-off procedure   (a) turn-on procedure   (b) turn-off procedure
Fig. 5. Proposed E-mode, cascode drive topology   Fig. 6. Proposed D-mode drive topology

For driving the D-mode GaN FET, the arrangement of the series resistor R_S and the parallel connection of the capacitor C and Zener diode Z_D are connected between the terminals of the input supply voltage of the isolated gate drive amplifier: V_{ISO} and G_{ISO}. The difference in arrangement between D-mode and E-mode is that for the D-mode GaN FET, one side of the series resistor R_S is connected to the positive terminal of the input supply voltage V_{ISO}, along with the parallel connection of the negative terminal of the capacitor C and the anode terminal of the Zener diode Z_D; the other side of the series resistor R_S is connected to the negative terminal G_{ISO}. The GaN source is then connected in the middle of the parallel connection of the capacitor C, Zener diode Z_D, and series resistor R_S, as shown in Figure 6. The operating procedure is outlined as follows: When the switch is turned on to provide the power supply voltage V_{DD}, the Zener diode Z_D clamps a voltage, V_{ZD}. Concurrently, the gate terminal with respect to the floating ground, G_{ISO}, is V_{ZD}. When the switch is turned off, the gate terminal with respect to the floating ground G_{ISO} is the voltage that the

Zener diode Z_D clamps, namely $-V_{ISO} + V_{ZD}$. Figure 7 shows the V_{gs} driving waveforms of proposed gate driver circuit before and after applying RCD circuit and the experimental waveforms.
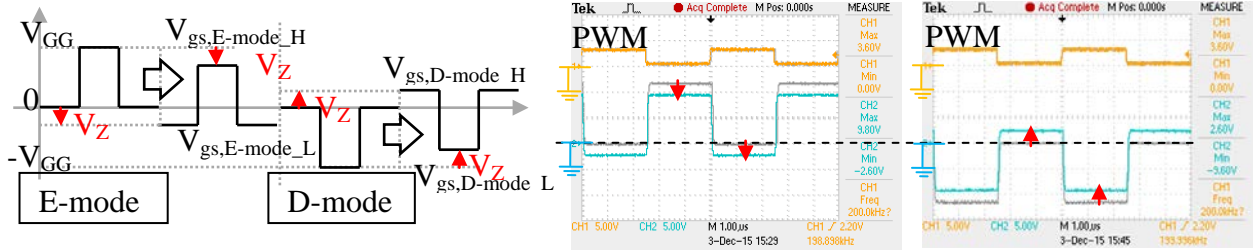
(a) Before and after applying the RCD circuit   (b) Experimental waveforms
Fig. 7. V_{gs} driving waveforms of proposed gate driver circuit (Left: E-mode / Right: D-mode)

Test results

Figure 8 illustrates plots of the AC capacitance waveforms. The off-state voltage, $V_{s(off)}$, value of the commercial cascode GaN FET was 2.2 V, as shown in Figure 8(a). The device turn-off resistance $R_{DS(off)}$ was 9.9 MΩ, as determined through the mechanism of isolated gate drive detection. The waveforms of different commercial cascode GaN FET samples were uniform, and the $V_{s(off)}$ value was maintained at 2.2 V, approaching the ideal isolated gate drive circuit detection signal. The relative parasitic capacitances were close to those specified on the datasheet; however, the commercial E-mode and fabricated cascode GaN FETs exhibited differences in voltage levels (within the 0–24 V range) between the gate and the ground. Figures 8(b) - (d) show three tested devices with large variations in $V_{s(off)}$, as well as their corresponding parasitic capacitances. For the commercial E-mode GaN FETs, $V_{s(off)}$ values of 1.2, 8, and 16.2 V were associated with $R_{DS(off)}$ values of 19.2 M, 2 M, and 481 kΩ, respectively. By contrast, for the fabricated cascode GaN FET, $V_{s(off)}$ values of 0.2, 11, and 23.6 V were associated with $R_{DS(off)}$ values of 119 M, 1.18 M, and 16.9 kΩ, respectively. These results reveal that the higher the $R_{DS(off)}$ values are, the closer are the parasitic capacitances to those specified on the datasheet. For the fabricated D-mode GaN FET, the variations in $V_{S(off)}$ values (within the 0–19 V range) were determined to be similar to the commercial E-mode and fabricated cascode GaN FETs. $V_{s(off)}$ values of 1, 11.6, and 19 V were associated with $R_{DS(off)}$ values of 23 M, 1.07 M, and 263 kΩ, respectively. Therefore, increasing $V_{DS(off)}$ widens the depletion region, while reducing $V_{DS(off)}$ strengthens the capacitive effect, and the drop voltage (V_{drop}) in capacitance moves farther from that specified on the relevant datasheet.
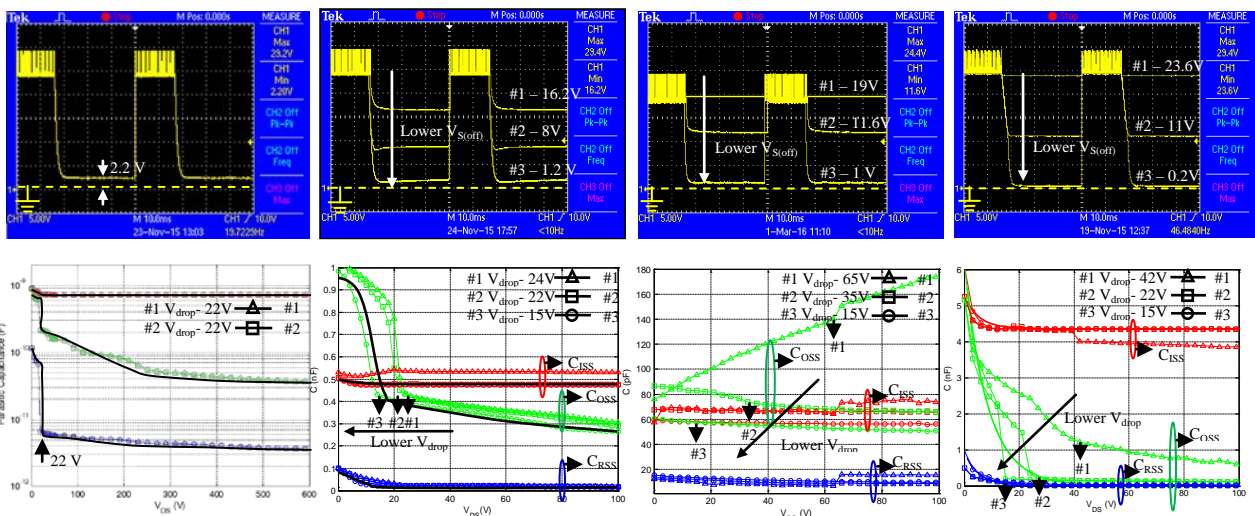
(a) Commercial cascode (b) Commercial E-mode (c) Fabricated D-mode (d) Fabricated cascode
Fig. 8. Relationship between GaN FET $R_{DS(off)}$ and parasitic capacitance

Table 1. Experimental property for GaN FETs in various modes.

GaN FETs / Samples		$V_{S(off)}$ (V)	$R_{DS(off)}$ (Ω)	V_{drop} (V)	C_{ISS}(pF) @100V	C_{OSS}(pF) @100V	C_{RSS}(pF) @100V	Electrical property
Cascode [5]	#1	2.2	9.9 M	22	722/740	106/133	5.45/3.6	Uniform
	#2	2.2	9.9 M	22	718/740	102/133	5.22/3.6	
E-mode [6]	#1	16.2	481 K	24	531	306	17.8	bad
	#2	8	2 M	22	476	289	16.9	
	#3	1.2	19 M	15	473/480	265/270	16.3/9.2	good
D-mode [4]	#1	19	263 K	65	74.2	175[*]	15.9	bad
	#2	11.6	1.07 M	35	65.8	65.6	9.34	
	#3	1	23 M	15	56	50.6	8.64	good
Cascode [3]	#1	23.6	16.9 K	42	3840[*]	548	2.3	bad
	#2	11	1.18 M	22	4350	114	1.87	
	#3	0.2	119 M	15	4350	110	1.84	good

([*] caused by large leakage current. Before slash: measured / After slash: datasheet)

Conclusion

This study applied parasitic capacitances and performed dynamic switching experiments to determine the relationships between device capacitance and turn-off resistance. These properties of GaN devices were estimated by adopting an isolated detection circuit used in a previous study, with the proposed gate driver topology. An isolated gate drive circuit could be utilized to drive E-mode, cascode, and D-mode GaN FETs. Relationships that can distinguish higher levels of device performance were established. The experimental results reveal that a GaN device with a lower $V_{S(off)}$ value exhibited a higher $R_{DS(off)}$ value, and therefore a higher voltage between the drain and the source ($V_{DS(off)}$). A lower $V_{S(off)}$ value is thus concluded to provide more accurate parasitic capacitance measurements.

Acknowledgement

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