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Research on Reconfigurable Instruments Based on FPGA

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Abstract. It is incidental for current automatic test system (ATS) to lead short of circuits, damage of instruments or units under test (UUT) by reason of its large amount of switches. To solve the problem, the technique of reconfigurable instrument is introduced. Using the reconfigurable instruments as substitutes for variety of single function instruments, the ATS reduces the number of switches, cuts down the redundancy of instruments and interfaces, improves reliability. By employing AP configuration mode, a FPGA partial reconfiguration scheme based on FLASH + SD card is introduced in this paper. The FPGA reconfiguration technology is analyzed and corresponding configuration SOPC system is designed. The reconfigurable instrument functions are realized combining the reconfigurable FPGA and universal peripheral circuits.

1. Introduction

The current common ATS uses switch system to allocate test resources. It causes a serious impact on system reliability and test efficiency because of the drawback with the high redundancy of instruments and signal ports, slow switching speed, easiness of short circuit or damage to the UUT. The Ai7 technology introduced by Teradyne, the famous instrument company, provided a new ATS framework based on universal signal ports. Under the new framework, every port has capability of all tests and stimulus without sharing resources with other ports through switch system. Accordingly, a lot of matrix switches and channel switches are saved, redundancies of instruments and test ports are reduced, and the system reliability is improved. And consequently, ATS construction, reduction and upgrade are all simplified, ATS maintenance and UUT test costs are reduced also.

For the new ATS framework, it is required that every port has the ability to provide different resources to different UUT, that is to say, every port has functions of a variety of instruments or is a reconfigurable instrument. Reconfigurable instrument is one of the key technologies of Next Generation Automatic Test System. Its hardware and software are changeable or reconfigurable by built-in configuration software after designed and manufactured or even in operation. Being able to reduce system size and power consumption, improve versatility and flexibility of the system, the reconfigurable instrument based on FPGA becomes one of important development directions of instrument technology.

2. Analyses on FPGA Reconfigurable Technology

FPGA with SRAM structure cannot maintain its configuration files itself. It needs an external nonvolatile memory as configuration memory, from which FPGA read configuration files to complete the configuration each time it powers on. Therefore, reconfiguration of FPGA can be realized just by changing the files in its configuration memory. That is this characteristic used by FPGA reconfigurable technology and making different logic functions realized in the same FPGA in the way of time division multiplexing (TDM).

FPGA reconfiguration can be divided into two models, the global reconfiguration and the partial reconfiguration. The global reconfiguration means the entire FPGA to be reconfigured and whole functions of the chip to be changed each time. The partial reconfiguration divides FPGA into two parts, the static zone and the reconfiguration zone. The former holds its logic functions and even keeps working while the latter being reconfigured. That achieves the dynamic partial reconfiguration. Comparing with the global reconfiguration, the partial reconfiguration has smaller

configuration files, faster speed, better flexibility and usability.
Fig.1 is block diagram of the dynamic partial reconfiguration. Various configuration files stores in the configuration module. To achieve the reconfiguration, the PXI controller sends commands though PXI interface and controls the configuration module to select corresponding configuration file, which is read by the FPGA through configuration port and sent to the reconfiguration zone.

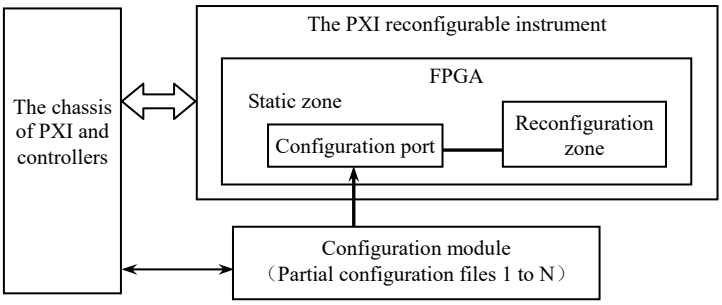

Fig.1. Block diagram of FPGA dynamic partial reconfiguration

3. The Scheme of Reconfigurable Instrument

Reconfigurable instrument are generally composed of reconfiguration core device and some function circuits. The instrument reconfiguration is to configure the core device. The function circuits are unchanged. Thus, it adopts universalized scheme generally. Fig.2 shows the block diagram of a multi-channel reconfigurable instrument based on PXI bus.

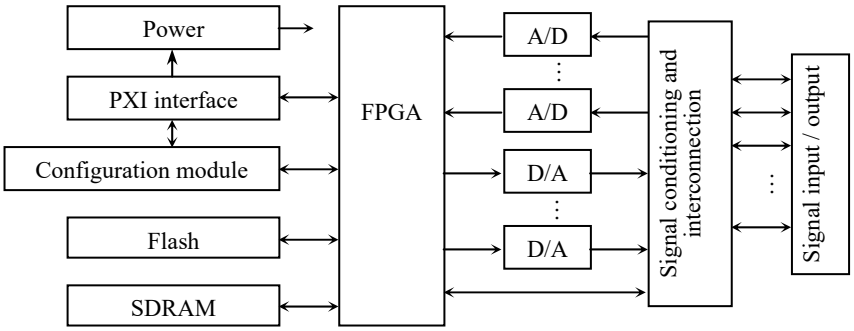

Fig.2. Block diagram of multi-channel reconfigurable instrument based on PXI bus

As shown in Fig.2, FPGA is the core device. Its internal circuit can be configured as processor system and various logic or control units of a reconfigurable instrument. It can achieve logic or control functions of multi-channel arbitrary waveform generators, digital voltmeters, frequency meters, edge detectors from different configuration files. The peripheral circuits of FPGA are mainly composed of a power supply module, a configuration module, PXI interface, SDRAM and Flash memories. The configuration module is composed of configuration memory and selection circuit of configuration files. PXI interface is measurement and control bus of the instrument, as well as reconfiguration channel of FPGA. The SDRAM and Flash are both external memories of FPGA and its internal configuration processor. The power module is a voltage converter, converting powers supplied by PXI bus to required voltages. The instrument functional circuits consist of A/D, D/A, signal conditioning circuits, etc., which are designed in universalized scheme. A/D takes basic signal acquisition. Combining with different FPGA configuration, it is able to achieve functions of digital voltmeter, oscilloscope even the spectrum analyzer, etc. D/A outputs basic analog signal. Based on FPGA configuration, it can realize function generator, arbitrary waveform generator and so on. The signal conditioning completes amplification or attenuation, filtering, level conversion of signals under test (SUT), to match test capability of A/D and D/A. The signal interconnection bus allots SUT to appointed test channels of the instrument, in order to reach capability of signal define for every test channel of the instrument.

4. FPGA reconfiguration mode

The early FPGA of Altera has mainly two configuration modes, the active serial configuration (AS) and the passive serial configuration (PS). The AS is controlled by FPGA. Its configuration memory is usually EPCS series chip. It is difficult for AS to meet the requirements of reconfigurable instrument, because of the limited programming number and the insufficient memory capacity of EPCS. The PS is controlled by external PC or controllers. It can configure the FPGA when the system is running. The PS controller can be selected variously, but relatively, its configuration sequence is complicated, configuration time is long and hardware circuit is difficult to debug.
The Altera Cyclone III FPGA series gives an active parallel configuration mode (AP), which uses FLASH as configuration memory. The AP can be realized by calling ALTREMOTE_UPDATE and PFL, Parallel Flash Loader, IP core in SOPC systems. It has uncomplicated circuit and high speed, supports multi-task reconfigurations and remote reconfigurations. Fig.3 shows its circuit structure.

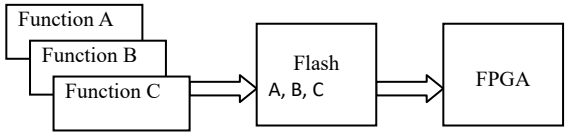

Fig.3. circuit structure of AP configuration mode

The AP can be operated in Quartus II platform by call ALTREMOTE_UPDATE and PFL IP core as well as user control logic writing in hardware description language (HDL). But the operation requires a deep understanding of the IP core and doesn't support the programs generated by SOPC system. So the operation is realized in this paper by employing Nios II software processor as controller and adding IP cores of ALTREMOTE_UPDATE, PFL and SD card controller to constitute a SOPC embedded system. Fig.4 shows the schematic diagram of the reconfiguration. Here, the Flash takes a role of buffer and the SD card stores reconfiguration files. So that, Users can quickly and easily erase existing files and update more files of configuration to make the instrument function selectable, reconfigurable and renewable for every channel.

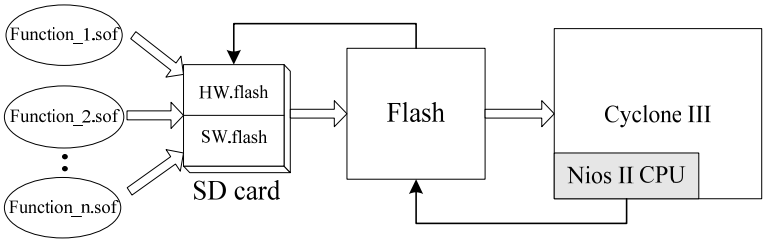

Fig.4. schematic diagram of AP mode by SOPC

5. Design of the Configuration Selector

The configuration selector enables users to quickly select, load, and run different configuration files on PC or the instrument controller. Its principle is to read the configuration file in specific address of Flash and reconfigure the SRAM of FPGA under the control of Nios II CPU, according to the AP of Cyclone III series of FPGA. It operates and scans all the configuration files stored in SD card when the system is powered up. After a function module is selected, it downloads the corresponding configuration file and software to Flash, resets and restarts FPGA automatically in succession, to run the function module. Fig.5 shows the block diagram of structure of the configuration selector.
Where, the three IP cores, Remote Update Controller, CFI Flash Controller and SD Card Controller, are key parts of the system. Component library of SOPC Builder provides the two formers. But the SD Card Controller needs to be composed by user.
The Flash is divided into multiple storage regions. The configuration information must contain a Nios II CPU whose address is 0. i.e., an initiator is contained at the address 0 of Flash. Its functions include refreshing Nios II instruction caches, refreshing Nios II instruction pipelines and jumping to

the Flash address containing function modules to load the corresponding configuration files and copy to the specified RAM to run.

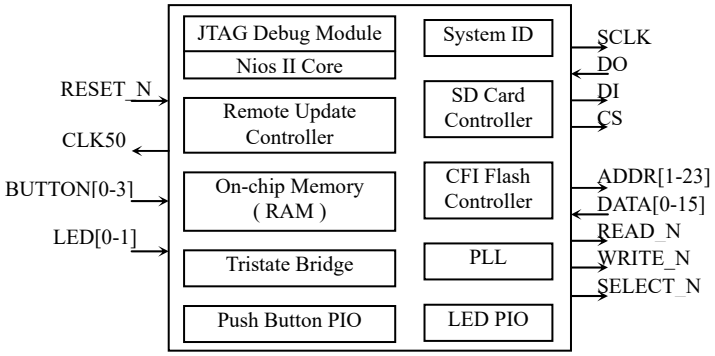

Fig.5. Block diagram of structure of the configuration selector

Configuration file of the configuration selector is stored in the region of Flash at address 0x20000 permanently. This is determined by AP configuration circuit of FPGA. The mirrors hardware configuration files of function modules store in the region addressing from 0x6800 to 0xE0000, where files with name of "<name>_hw.flash" are loaded from SD card by the configuration selector in order to configure the FPGA.

The Flash also stores software files. If the function module is a SOPC system, the software mirror file of the configuration selector should contain a booting procedure, to boot the codes in function module's software files to be copied to specified RAM to operate. The booting procedure will be automatically added into the Flash files when it is converted into Flash file by ELF2, the Flash converting software. Software procedures of the function modules store from address 0x28000. The storage is required not to exceed 4M bytes.

6. Realization of Reconfigurable Instrument

The function circuits of reconfigurable instrument are universal. The key to reconfigure instrument is the partial reconfiguration of FPGA, or the SOPC system of configuration selector.

6.1 Construction of the SOPC system

In SOPC Builder environment, the SOPC system can be constructed as follow: To add and configure IP cores resources according to the requirements of the configuration selector; to connect these resources by Avalon Switch Fabric bus; to assign base address for each component by the Auto-Assign Base Address; to set interruption priorities for the slave devices with interrupt request by Auto-Assign IRQ. Address and interruption assignments of the SOPC system are shown in the Fig.6.

Use	...	Module Name	Description	Clock	Base	End	IRQ
☑		cpu	Nios II Processor	cpu_clk	0x09000800	0x09000fff	
☑		flash_ssram_pipelin...	Avalon-MM Pipeline Bridge	cpu_clk	0x0c000000	0x0dffffff	
☑		pipeline_bridge_befo...	Avalon-MM Pipeline Bridge	cpu_clk	0x00000000	0x01ffffff	
☑		flash_ssram_tristate...	Avalon-MM Tristate Bridge	cpu_clk			
☑		sram_512x16bit	SRAM_512x16bit	cpu_clk	0x01000000	0x010fffff	
☑		ext_flash	Flash Memory (CFI)	cpu_clk	0x00000000	0x00ffffff	
☑		cpu_ddr_clock_bridge	Avalon-MM Clock Crossing Bridge	multiple	0x00000000	0x03ffffff	
☑		ddr_sdram	DDR2 SDRAM High Performance Contr...	osc_clk	0x00000000	0x03ffffff	
☑		slow_peripheral_bri...	Avalon-MM Clock Crossing Bridge	multiple	0x08000000	0x087fffff	
☑		sys_clk_timer	Interval Timer	peripheral_...	0x00000100	0x0000011f	8
☑		performance_counter	Performance Counter Unit	peripheral_...	0x00020000	0x0002001f	
☑		jtag_uart	JTAG UART	peripheral_...	0x00002000	0x00002007	10
☑		sysid	System ID Peripheral	peripheral_...	0x00000200	0x00000207	
☑		button_pio	PIO (Parallel I/O)	peripheral_...	0x00004000	0x0000400f	12
☑		led_pio	PIO (Parallel I/O)	peripheral_...	0x00005000	0x0000500f	
☑		pll	PLL	osc_clk	0x00200000	0x0020001f	
☑		sd_card_controller	SD/MMC-Card SPI Interface	peripheral_...	0x00620000	0x0062001f	18
☑		remote_update	Remote Update Controller (Cyclone III)	remote_up...	0x00610000	0x006100ff	

Fig.6. Address and interrupt assignments of the SOPC system

6.2 HAL-based software design

Hardware Abstraction Layer or HAL is the base of Nios II software architecture. Its library supplies hardware driver interfaces for the devices to interact with applications. To achieve the purpose of reconfiguration, the applications can call corresponding drivers in the library to control the hardware according to their specific function requirements. Fig.7 shows the workflow of the configuration selector.

7. Conclusions

Based on analysis of reconfigurable technology of FPGA, using the AP configuration, a FPGA partial reconfiguration scheme based on "Flash+SD card" is designed and the corresponding configuration selector SOPC system is constructed. And further more, the reconfigurable instrument is implemented by combining the reconfigurable FPGA and universalized external function circuits. The configuration selector SOPC system runs automatically when it powers up. It calls the standard components ALTREMOTE_UP-DATE and PFL in SOPC library and the user designed SD card controller IP core, to load configuration files and reconfigure the FPGA. The AP-based FPGA reconfiguration has the advantages of convenient use, high integration, reliable data transmission, easy remote upgrade and maintenance, and is successfully applied in the design of the reconfigurable instrument proposed in this paper.

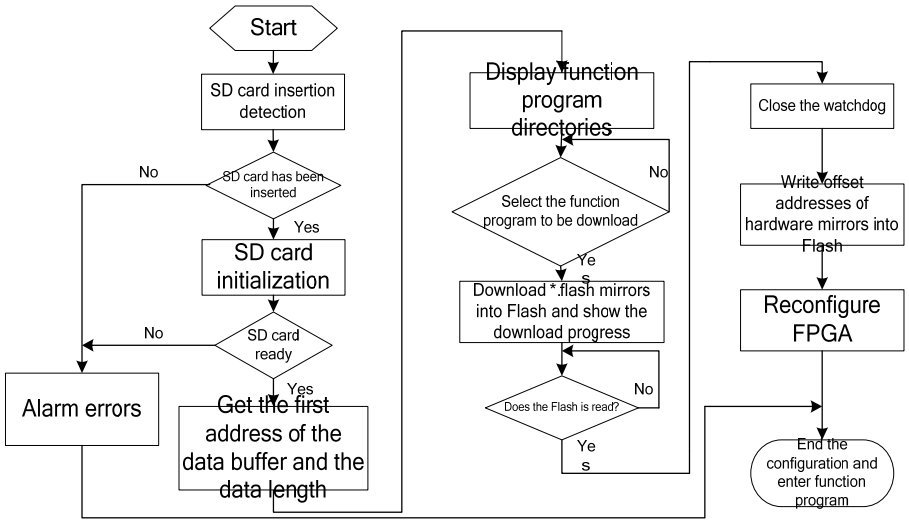

Fig.7. Workflow of the configuration selector

References

[1] ZHANG Wen-quan, *Research on Reconfigurable Analog Test Instrument Technology*. Shijiazhuang: Shijiazhuang Mechanical Engineering College, 2011.10.

[2] Fu Zhenpeng. *Research on PXI Reconfigurable Instrument for Missile Tests*. Harbin: Harbin Institute of Technology, 2014.6.

[3] ZHANG Wen-quan, CUI Shao-hui, CHEN Jian-si. Application of FPGA Configuration on Reconfigurable Instrument Based on AP. *Computing Technology and Automation*, 2011.9, Vol.30, No.3.

[4] ZHANG Wen-quan, CUI Shao-hui, CHEN Jian-si. Design of a Reconfigurable Multi-purpose Instrumment Based on FPGA. *Computer Measurement & Control*, 2011.19(10).

[5] Kumm M, Moller K, Zipf P. Reconfigurable FIR filter using distributed arithmetic on FPGAs, 2013 IEEE International Symposium on. IEEE, 2013: 2058-2061.

[6] Information on http://www.altera.com/