Circuit System Design Based on FPGA Configuration

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Abstract. With the development of microelectronic technology, the chip performance o FPGA becomes more and more powerful. This paper firstly introduces the concept of FPGA, then analyses three principles the designer must follow, and finally gives the basic flow of the circuit system design based on FPGA configuration to provide some references for the related researchers.

Concept of FPGA

FPGA (Field-Programmable Gate Array) is the further development product of the CPLD (Complex Programmable Logic Device) and other programmable devices. As an a semi-custom circuit of the field of Application Specific Integrated Circuit (ASIC), it not only solves the lack of custom circuit, but also overcomes the shortcoming of finite original programmer gates of circuit.

FPGA is a kind of programmable logic device, which is composed of tens of thousands of identical programmable logic units. After manufacturing is completed, the FPGA can be programmed at the job site in order to achieve specific design features. The typical design work includes the simple logic function of each unit, and selectively closes some of the switches in the interconnection matrix. In order to ensure the normal operation, FPGA must use the appropriate power management technology. FPGA was originally used for system prototype production, the final production will be replaced by high speed IC or ASIC. However, in recent years, the performance of FPGA has been greatly improved. FPGA is now widely used in production design as the cost is declining. The power dissipation of FPGA depends on many different factors, closely related to the design. Accurate power estimation methods must be used to ensure that the power supply system meets the FPGA requirements. FPGA manufacturers provide network tools for power consumption calculation. In order to estimate the power consumption of FPGA, the calculation procedure should consider the design resource utilization, the switching speed, the working clock frequency, the I/O usage and many other factors. There are three main configurable components in FPGA. They are Configurable Logic Module (CLB), I/O Module (IOB) and Interconnect. Among them, CLB provides functional logic elements and IOB provides the interface between the package pins and the internal signal lines. The interconnect resources provides routing paths to connect the input and output of IOB and CLB.

Design Principles of Circuit System Based on FPGA Configuration

Principle of Pipeline Design. The principle of pipeline design is to segment a long path into several small paths via the register like a pipeline so as to improve the working speed. Assuming the original path delay is t, adding 2 level pipeline and assuming that the path is divided evenly, then the path delay can be reduced to about t/3, thus the system rate can be increased to 3 times the original. Of course, it should be noted that the output will be delayed by 3 clock cycles, so just use assembly line technology, remember to adjust the timing. We consider a circuit each clock cycles to

execute N operations and the operating frequency is F. We can know that the throughput of the system is N*F ops/sec. The nature of the pipeline is to improve the throughput by increasing the F, making the trade-off situation of latency and area. The sketch map of the pipeline design principle is shown in Figure 1.
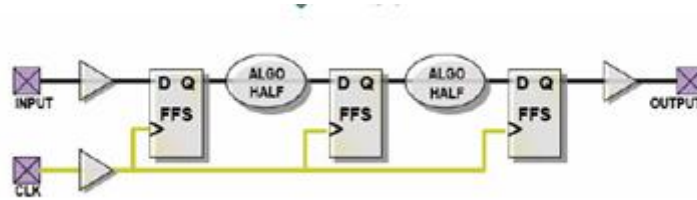

Figure 1.Sketch map of pipeline design principle

Principle of Asynchronous Clock. In the digital circuit, the clock is the most important signal of the whole circuit. The clock signal is usually the most important signal of the load, so the load should be reasonably distributed. The best clock scheme in the FPGA design is: a dedicated global clock input pin is used to drive a single master clock to control every trigger in the design project. When we do the synchronous design, the global clock input is generally connected to the clock side of the device. Otherwise, it will be affected by its performance. For the need for multiple clock timing circuit, it is best to choose a frequency is their high frequency of the clock frequency of the main clock. Many systems require multiple clocks in the same design, and the common example is the interface between the two asynchronous microprocessors, or the interface between the microprocessor and the asynchronous communication channel. Since the two clock signals are required to establish and maintain time, the application introduces the additional timing constraints, which will require synchronization of certain asynchronous signals. The principle of asynchronous clock is shown in Figure 2:
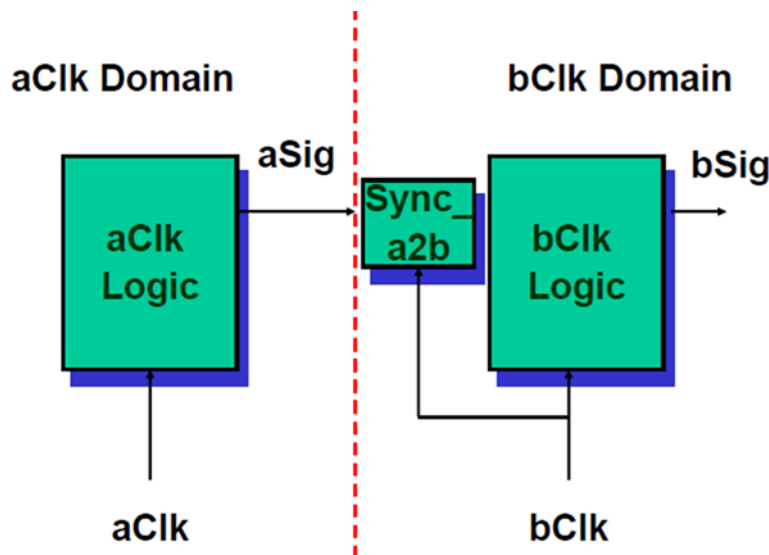

Figure 2. Asynchronous clock model

Principle of Removing Burrs. Some situation will lead to the burrs, such as the competition, the adventure, delay of routing and the coupling of signals. We use the gray coding in the state machine which can avoid the bus at the same time in a clock cycle in the bit flip and lead to the burr. This code can be used as a counter in the chart above. Gray code in any adjacent two groups of code, there is only one digital. Gray code method is also a common way to reduce the power consumption of the design, because it reduces the level of the register. The use of gray code counter, synchronous circuit, can greatly reduce the burr, but it cannot completely eliminate the burr. The data input end

of the register D makes the burr insensitive in the clock EN. Therefore, we can use D to absorb the burr signal, which is shown in the Figure 3.
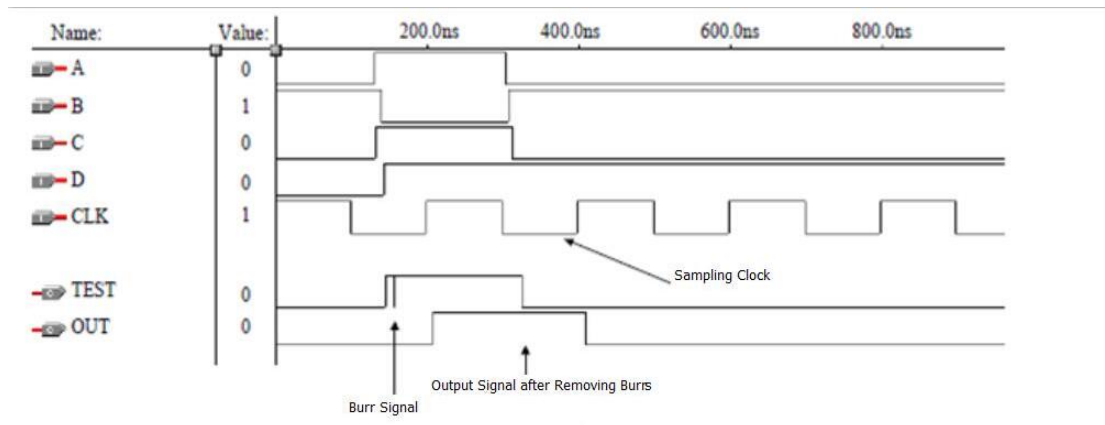

Figure 3. Process of removing burrs

Design Flow of Circuit System Based on FPGA Configuration

Function Design. The first thing before the system design is to do the preparation work, such as the program demonstration, system design and FPGA chip selection. According to the requirement of the task, the system engineer trade-off selection reasonable design scheme and suitable device type considering the complexity, the working speed and the chip. We generally use the top-down design method. The system is divided into several basic units. Each basic unit can be divided into the next level until the EDA component appears.

Input Design. Input design is the design process of developing software to express the system or circuit and input it to the EDA tool. The commonly used methods are hardware description language and schematic input method. Schematic input method is one of the most direct descriptions of the development of the early application of programmable chip. It will be required for the device from the component library to tune out. This method is intuitive and easy to simulate, but the efficiency is very low, and it is not easy to maintain. It is not conducive to the construction and reuse of modules. The main drawback is that the portability is poor, when the chip upgrade, all the schematic need to make some changes. At present, the most widely used in practical development is the hardware description language input method to support the logic equation, the true value table and state machine. The two languages are standards of the Institute of electrical and Electronics Engineers. Their common features are language and chip technology independent, conducive to top-down design, easy to module partition and transplantation, transplantation with strong logical description and simulation function, and the input efficiency is very high. Function simulation, also known as the former simulation, is the logic function of the circuit designed by the user before the compiler verification. Although functional simulation is not a necessary step in the process of FPGA development, it is the most critical step in the system design.

Simulation Design. In order to be able to be converted into a standard gate structure, the program must be written in a style that meets the requirements of a particular synthesizer. Due to the gate level structure, the program synthesis is a very mature technology. All of the integrated devices can support the integration of this level. After synthesis, the simulation results are consistent with the original design. In the simulation, the integrated generated standard time delay file is labeled to the integrated simulation model, which can estimate the impact of the gate delay. However, this step cannot be estimated line delay, and there is a certain gap between the actual situation and the wiring is not very accurate. The synthesis tool is more mature, as the design of the

general can omit this step. If you find the wiring layout found in circuit structure and design intent do not match, you need to back to the comprehensive simulation to confirm the problem. Software tools introduced in the functional simulation generally support the integrated post simulation.

Wiring Design. Implementation is the integrated production of the logical network table configuration based on FPGA. The wiring design is the most important process. The layout of the hardware and the underlying elements of the logic network table are reasonably configured to the inherent hardware structure of the chip, and often needs to make a choice between the speed and the area of the best. According to the layout of the topology, wiring design uses a variety of connections within the chip resources and some reasonable and correct connections of the various components. At present, the structure of FPGA is very complex, especially when there is a time sequence constraint using the engine to make the layout and routing. After the end of the wiring, the software tool will automatically generate reports to provide information on the design of the various parts. As the FPGA chip manufacturer is the most familiar with the structure of the chip, the wiring tools should be developed by the chip manufacturer.

Conclusion

The good features determine that FPGA configuration will be applied widely in the field of circuit system. This paper introduces the concept and characteristics of FPGA configuration and the design principles of it. Then, we explore the design process of circuit system based on FPGA configuration. However, due to the limit ability and time, some problems, such as actual cases and design details need further study.

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