Design of Handheld Oscilloscope Based on FPGA and Dual A/D

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Abstract. Handheld oscilloscope because of its portability, wide application range and other characteristics, has drawn more and more attention in the engineering practice. Anolog-to-digital conversion circuit plays an important role in the design of digital oscilloscope. It directly determines the maximum frequency of digital oscilloscope can be measured. This paper focuses on the analysis of three methods of improving the sampling rate, eventually adopts double anolog-to-digital converter sampling approach to the design of a handheld oscilloscope, sampling frequency can reach two times the maximum sampling frequency of anolog-to-digital converter, so as to improve the accuracy of frequency measurement range of oscilloscope and the waveform display, and without significant increase in cost and easy to realize. The oscilloscope with embedded processor STM32 as control core, using Field－Programmable Gate Array (FPGA) for data processing. The signal collected by automatic gain control, dual anolog-digital converter sampling,data cache, digital-to-anolog conversion process, displayed on the screen. At the same time ,the oscilloscope realizes the functions of test signal's display, measurement and the corresponding parameter adjustment. *Copyright © 2014 IFSA Publishing, S. L.*

1. Introduction

With the development of information technology, the oscilloscope has been used more and more widely, but people also put forward higher requirements on the performance of the oscilloscope. With a high sampling rate, high resolution and low error, low cost and high performance digital oscilloscope has a very high demand in the market. The sampling frequency of anolog-to-digital converter(ADC) directly affects the output frequency of the digital frequency synthesis technology. At present the high sampling rate of the ADC chip as the price is expensive, and not widely used, therefore, how to improve the sampling rate based on the existing ADC has become one of the research directions of people. In this paper, the design of a handheld oscilloscope adopts double anolog- to-digital(A/D) sampling mode, is very good realization of low cost and high sampling rate requirements, has good application prospects in signal measurement.

2. Three Methods of Improving the Sampling Rate

According to the Nyquist theorem [1], the sampling frequency is at least 2 times the highest frequency of the measured signal. In fact, it is very difficult to accurately restore the original signal at two times the frequency of the highest frequency of the signal to sampling, it is usually adopts 5 times or even 10 times the signal frequency to sample. Therefore, this requires A/D converter has a high conversion rate.

Due to technological limitations, single A/D chip's sampling rate and precision can not be very high at the same time. If you want to achieve a higher sampling rate and accuracy, it needs to take certain measures. Mainly in the following three ways

2.1. Double ADC Synthesis Technology of Using High Speed Switching

The technology uses two of the same model ADC, in a set-up time for a total of two samples, high-speed switching at twice the frequency of the sampling clock gating two ADC, in order to achieve double the sampling rate [2].The advantage of this solution is the use of a relatively inexpensive high-speed switch, to achieve the purpose of increasing the sampling rate. Figure 1 is the use of high-speed switching of dual A / D synthesis schematic.

Fig.1. Double ADC Synthesis Technology of Using High Speed Switching

2.2. Quadrature Mirror Filter Bank and Hybrid Filter Banks ADC System

Based on the basic idea of quadrature mirror filters (QMF) of ADC system are: the input analog signal time discretization [3] and then use discrete-time decompose filter based on switched capacitor filtering the signal, through the upsampler, quantizer and downsampler, then using digital synthesis filter anti-aliasing and digital signal synthesis [4]. Figure 2 is based on QMF's M-channel ADC systems. $\uparrow_M$, Q , $\downarrow_M$ respectively upsampler, quantizer and downsampler.

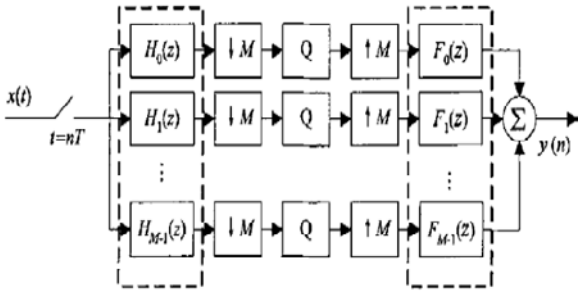

Fig.2. The ADC system based on QMF

The ADC system based on QMF can achieve high sampling rate of the A/D conversion,by a plurality of low sampling rate ADC, but switched capacitor introduced switching noise, and the switch structure also limits the speed of the ADC system. In order to solve this problem, S.R.Velazque proposed a hybrid filter banks(HFB) based on ADC system. The basic principle of ADC system based on HFB: the use of the analog analysis filter converts the analog input signal is decomposed into several frequency bands of equal bandwidth, the signal of each frequency band were also sampled with a low ADC, digital synthesis filters can eliminate the spectrum sampling caused by aliasing, realizing approximate signal reconstruction [5]. Figure 3 is ADC systems based on HFB.

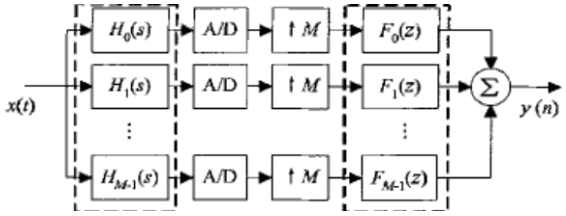

Fig.3. The ADC System Based on HFB

The ADC system based HFB has some notable features: adopting a unified system clock, which can avoid errors due to differences arising from various quarters. RLC circuit simulation using decomposition filters, switched capacitor circuits to overcome the limitations of the effective number of bits of the system.

2.3. Using the Clock Divider for Multi A/D Parallel Sampling

The clock divider distributes the same clock to different A/D as a clock input, but every clock output has different phase. It can be realized by using the phase shifter or precision delayer [6]. Figure 4 is the schematic of using phase shifter to achieve multi ADC parallel sampling.

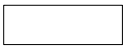

Fig.4. The Schematic of Using Phase Shifter to Achieve Multi ADC Parallel Sampling

The above three methods to improve the sampling rate of each have advantages and disadvantages. Scheme 1: the use of dual ADC synthesis technology of high speed switching scheme is easy to implement, but must use rate of electronic switch with high speed and high quality, and the system reliability and maintainability put forward higher requirements; scheme 2: unified clock with ADC system of hybrid filter banks based on the recovery plan, avoid the error produce various clock difference, overcome the limit switch capacitor circuit on the effective number of bits of the system, but the application of this technology development and design of the ADC system there are many problems have not been solved yet, not easy to realize; scheme 3: using the clock divider realize multi A/D parallel principle of sampling scheme is relatively simple and easy to implement, but when the sampling rate is too high the requirements of this principle, the phase shifter or delay is very high.

Considering the easy realization and practicability, this design uses the 3th scheme, using double A/D converter sampling, realize sampling rate multiplication.

2.4. Dual A / D Converter Sampling Theory

Using the clock divider realize multi A/D parallel sampling to improve sampling rate is a method of comparative economic efficiency, using dual A/D converter, without significantly increasing delay device requirements, can be very good to achieve the purpose of sampling rate multiplication. This design uses two 8 bit high speed anolog-to-digital converter ADS830E of TI company, the sampling frequency is 10 kSa/ for s~ 60 MSa/ s. Figure.5 is ADS830E's timing diagram.

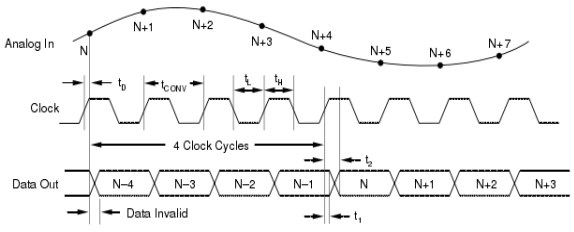

Fig.5. Timing Diagram of ADS830E

High-speed analog- to-digital converter module we use two alternate sampling ADCs work, Field－Programmable Gate Array(FPGA) produces two phase difference of ninety degrees from the pulse clk1 and clk2, which are used to control two A/D converters. Thus the two ADCs can work simultane-ously to ensure an ADC sampling, the other ADC during the conversion, so A/D module overall data hold time will be reduced by half, then realized the sampling frequency increases times, the maximum sampling rate of up to 120 MSa/s. Work is shown in figure 6

Fig.6. Dual A/D Sampling Principle

Clock generation circuit composed of A/D converter provides a series of sampling clock signal, the sampling frequency of 8 stalls: 600 Sa/s, 6K Sa/s, 60 kSa/s, 600 kSa/s, 1 MSa/s, 6 MSa/s, 30 MSa/s, 60 MSa/s; The sensitivity adjustable button to achieve horizontal scanning velocity and vertical voltage [7].

3. The Overall Design of the Hardware

The handheld device with a high-performance oscilloscopes, low-cost, low-power embedded processors STM32 for display and control center systems. ALTERA FPGA processor of choice is produced by Cyclone IV series EP4CE15 chip, which has a powerful data processing capability, and crystal, power supply and other simple peripheral circuit,

constitute a system of data storage and processing centers. Plus programmable amplifier circuit controlled by the STM32, ADS830 analog-digital conversion circuits and CAT4237 chip-based TFT backlight driver circuit constitutes the entire handheld oscilloscope design. The overall design of the system block diagram shown in Figure.7.

Fig.7. Overall System Design Diagram

Analog signal first enters the automatic gain control(AGC) circuit, the signal amplification/ attenuation within a certain range, and then into the double anolog-to-digital converter circuit for signal sampling. After processed by anolog-to-digital convert, data are deposited inside the FPGA input First Input First Output Memory (FIFO), after processed by sine interpolation algorithm, data are sent to the output FIFO, when FIFO is full, STM32 begin to read from the FIFO. The data through waveform processing will be displayed on the TFT display.

3.1. The Design of the Signal Conditioning Module

Firstly, signal conditioning circuits process analog signals, and then sent to double A/D sampling module. Signal conditioning circuits AC/DC coupling selection and programmable attenuator selection effect. Conduction through the control relay or not to implement the AC/DC coupling selection, magnetic latching relay selection relays, magnetic latching relay switch pulls

in current consumption is less than ordinary relays in general, is very suitable for low-power handheld instrument use.

STM32 outputs a control signal to the relay of the default input signal 100 times attenuation. The attenuated signal after A/D conversion in the STM32 collected, and the preset gear determination thresholds, and if the signal amplitude is too low, STM32 adjustment control signal to reduce the attenuation factor of the input signal, that the attenuated signal reaches the optimum measurement range. Because the resistance inductance effects at high frequencies, so the attenuation resistor in parallel across the capacitor as a high frequency compensation.

The attenuated signal into the THS4082 consisting voltage follower having a high input impedance, the output impedance characteristic is small, the voltage signal remains unchanged.

3.2. Automatic GainControl(AGC) Circuit

AGC circuit of the compression ratio can be automatically controlled by changing the magnitude of the gain of the input and output, expanding the range of the receiver, it is possible to change the input signal amplitude is large, the amplitude of the output signal is kept constant, or only to a lesser extent the change, not because the input signal is too small or too large can no longer good on the display. This paper designs consisting of programmable amplifier AD603, using the official datasheet recommended program, as shown in figure 8.

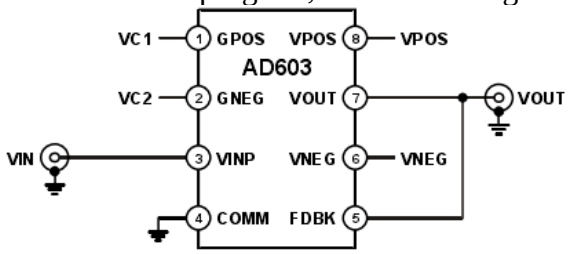

Fig.8. -10 dB to +30 dB; 90 MHz Bandwidth Programmable Amplifier

Through a low-power, 12-bit voltage output DAC chip TLV5618A to control vc1, vc2, the voltage difference between the two ports to change the relationship between the gain of the amplifier gain and the voltage difference ,$Gain(\text{dB}) = 40V_G + 10$, $-500mV \le V_G \le +500mV$. Amplifier within 0 ~ 90MHz band has -11dB ~ 31dB of amplification.

4. Data Processing and Control

4.1. FPGA Data Processing Module

In this design, the main function of FPGA is to control the ADC and DAC and the high speed data stream buffer for ADC. Using ALTERA's built-in IP kernel, can easily achieve the desired function. Specific modules need programming including PLL system clock generating, FIFO data cache, STM32 interface and A/D clock control module. The PLL module for the system clock module, A/D, clock control module through the control signal is given by the STM32 to adjust the output frequency division ratio sampling rate through this way to regulate A/D.

4.2. Design of STM32 Host Controller

STM32 as the display and the control center of the system, the user can through the button to adjust the waveform oscilloscope, signal acquisition, waveform control parameters of data acquisition, waveform parameter measurement, waveform data processing, display driver, follow-up data communication function. When the button is pressed, the system enters the interrupt. Corresponding to different keys, we set up the corresponding interrupt number. System interrupt number judgment first in the interrupt processing, and then transferred to the corresponding response procedures for specific adjustment.

The concrete work flow of STM32: first of all, power system, initialization.When FPGA's FIFO is full, notify the STM32 to close the FIFO, then read the data from the FIFO, the read-out data through the digital-analog conversion, according to the numerical size one by one point on the TFT screen tracing point. As a result, data is displayed on the TFT screen, because the data is discrete, in each time interval increases oscilloscope lattice will appear

discontinuous phenomenon, where the use of method of sine interpolation, restore out by sampling the signal waveform is more accurate.

4.3. Sinc Interpolation Algorithm for FPGA Implementation

The system uses FPGA to achieve the overall structure of the sine interpolation block diagram shown in Figure 9, including input and output FIFO module, logic control and frequency processing module, ROM lookup table module and multiplier-accumulator MAC module.

The input data is through double A/D sampling data, under the control of write clock and read clock, the data are stored in the input FIFO. The logic control and frequency processing module is the design of central control module, it is mainly to complete the input data sampling process, but also control of input and output of data storage and read, produce ROM lookup table read enable signals and address signals [8].

Fig.9. Structure Diagram of Sinc Interpolation

It is based on the input FIFO full/empty flag to decide whether to continue to store the data or the data read from the in. If no input data in the FIFO, then the system stored data to it; if there is data in the input, the system reads from waveform data and also produce a read enable signals and address signals to the lookup table in the system clock under the action of the lookup table will be based on the effective read enable signals and address signals, addressing to have been deposited in the interpolation coefficient, produce corresponding interpolation coefficient. Also in the system clock under logic control and frequency division processing module will increase the sampling data and the interpolation coefficient after sampling into MAC multiplication accumulation module carries out the interpolation calculation, the calculating results are stored in the output cache in FIFO. The logic control and frequency processing module is also based on the output space full flag on the output to read write control and generate corresponding read / write enable signal, and control the output of the read and write [9].

4.4. User Interface Design

To provide the user-friendly interface, this design transplant UCGUI user interface system. UCGUI is Micrium company produced a open source code for embedded systems excellent graphics software applications provide efficient processor and LCD controller-independent graphical user interface to any use of LCD graphic display it. Suitable for single-task system or a multi-task environment, and is applicable to any arbitrary size of the real and the virtual display at the LCD display controller and CPU. UCGUI can be more convenient to use the graphical interface of the system and can be designed to be very intuitive waveform signal processing and display. Then transferred to the corresponding response program of specific adjustment.

5. Conclusion

This paper analyzes the three ways to improve the sampling rate, finally adopts double A/D sampling scheme gives the implementation method of handheld oscilloscope, achieve the purpose of doubling the sampling rate, and no significant increase in cost and easy to realize; using sinc interpolation algorithm to make the final display waveform continuity has been greatly improved; by using combination of FPGA and STM32, making this design have a high performance space and the reference value.

On the final physical results showed that this design is able to below 1MHz, above 10mV waveform without distortion of the display. Figure 10 is a frequency of 5kHz, peak-to-peak 500mV sine wave display results, waveform display good, basically no distortion.

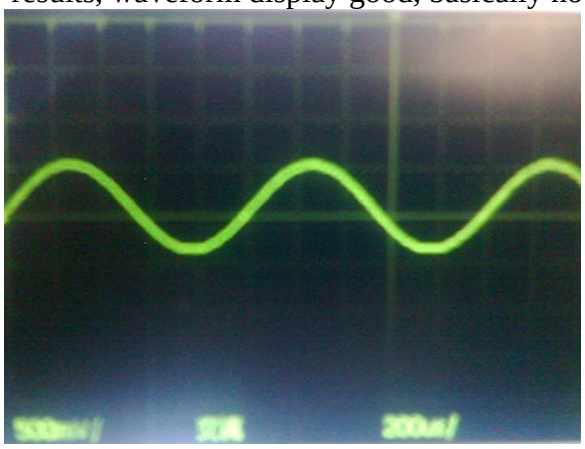

Fig.10. Actual Oscilloscope Waveform

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