

# A Negative Output Low Dropout Voltage Regulator with Quiescent Current Reduction

Wentao Liu <sup>a</sup>, Jie Zhang and Maomao Sun

Sichuan Institute of Solid State Circuits, Chongqing, China.

<sup>a</sup>went2013@sina.com

**Abstract.** This paper presents a low-dropout regulator with quiescent current reduction. The quiescent current reduction circuit can change the Darlington Driver to the emitter follower at large dropout-voltage. The proposed LDO can output a steady voltage of -5V as the input voltage varies between -5V to -26V. The LDO with the proposed structure has been implemented in a 40V high voltage bipolar process. It is able to deliver up to 1A load current and only dissipates 1mA quiescent current at large dropout-voltage.

**Keywords:** Quiescent current reduction; Negative output; LDO.

## 1. Introduction

Power management has become an important research area in both, battery and hand-held electronic products, as the consequence of the limited energy [1, 2]. In many areas, the low power consumption system such as low dropout regulators (LDO) play an important role under large variations of input voltage. There are so many researches in low power consumption LDO to reach the goal of long standby time of the electronic system [3~5].

A LDO with negative voltage output is proposed in the paper, which performs low quiescent current. It can offer load current in excess of 1A, with the typically dropout voltage of 0.6V, while its quiescent current can be as low as 1mA.

This paper describes the design and the implementation of a low dropout regulator with low quiescent current in 0.6μm high voltage bipolar technology. Section 1 introduces the design briefly. Section 2 discusses the traditional structure of the negative regulator and design challenges for low power consumption. In Section 3, the proposed circuit is discussed, and the simulation results are given. Finally, the experimental results and conclusions are addressed.

## 2. Traditional structure

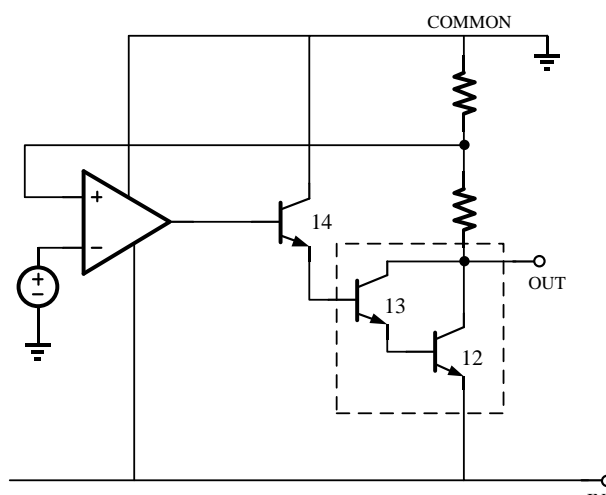


Fig. 1 Simplified block diagram of negative-voltage regulator

By reversing the appropriate voltage polarities and using the high-current pnp transistors as the power transistors, we can apply the basic voltage regulator principle to negative regulator. However, in monolithic design, this idea is not available. A more commonly used way is using the Darlington

npn power transistor, which will improve the effective gain, as shown in Fig. 1. Noted that the Darlington structure introduces the third gain stage into LDO, which may cause the frequency compensation more difficult in heavy load. The Darlington structure also involves a phase inversion of the error signal, so the sample voltage  $V_s$  is now connected to the non-inverting input of the error amplifier [6].

As Fig 1 shows, the circuit controls the conduction in transistor Q1 so that the output voltage is at the setting level regardless of the input voltage or the load current. Q2 and Q1 make up the Darlington structure. Q7 acts as an emitter follower controlled by amplifier to operate the Darlington.

The voltage regulator of Fig 1 plays an important role, but its dropout voltage, given by Eq 1, is limited to the  $V_{BE}$  of Q1 plus the  $V_{SAT}$  of Q2. This is typically about 1V.

$$V_{Dropout} = V_{be_{Q1}} + V_{SAT_{Q2}} \approx 1V \quad (1)$$

If lower dropout is desired, Q2 can have its collector return to ground thus turn the Darlington to an emitter follower driven common emitter transistor. However, in such a configuration, the current flowing in Q2 will increase the regulator quiescent current and is therefore undesirable.

### 3. Improved structure

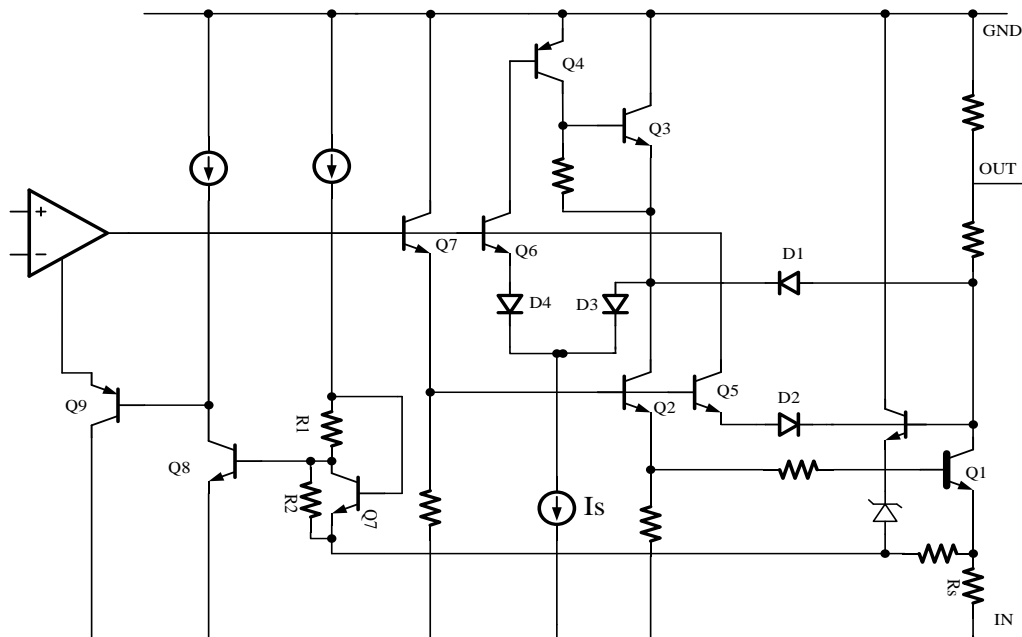


Fig. 2 Proposed quiescent reduction circuit

#### 3.1 Description of the circuit

In the schematic diagram of Fig. 2, the new circuit is shown. A number of elements carry the same designation as those of Fig. 1. These elements perform similar functions. For example, transistor Q1 is the output transistor. Q2 is the driver of Q1. There is a phase resistor about 50 ohms in series with Q1 which acts as the current limiting resistor.

#### 3.2 The quiescent current switch inside the circuit

If the output voltage is about 5V above the input voltage, then the collector of Q2 is a  $V_{be}$  below the collector voltage of Q1, which will conduct D1. When D1 is conducted, driver Q2 will be Darlington connected to Q1. In this case, the current source will get into D3. So, D4 will turn off. As the result, no current flows into the base of Q6, so the branch of Q4 and Q3 will turn off.  $I_s$ , typically, will be 80  $\mu A$  and will represent a relatively small percentage of the current flow in D1. Under this condition it can be seen that the output of the error amp will be about triple of  $V_{be}$  above terminal IN.

If the output voltage slowly falls down, the voltage at collector of Q2 is reduced. When the dropout voltage is about 3  $V_{be}$ , both D4 and D3 will conduct current to the current source  $I_s$ . As the result, Q6 will turn on, which will make Q3 and Q4, the composition PNP structure, sourcing current to Q2. As

the dropout voltage goes lower than  $3 V_{be}$ , the voltage drop across D3 becomes less which turn D3 off and D4 turn on. Finally, when the dropout voltage is about  $2 V_{be}$ , almost all the current of  $I_s$  comes from D4. Then, Q6 pulls about  $80\mu A$  from the base of transistor Q4.

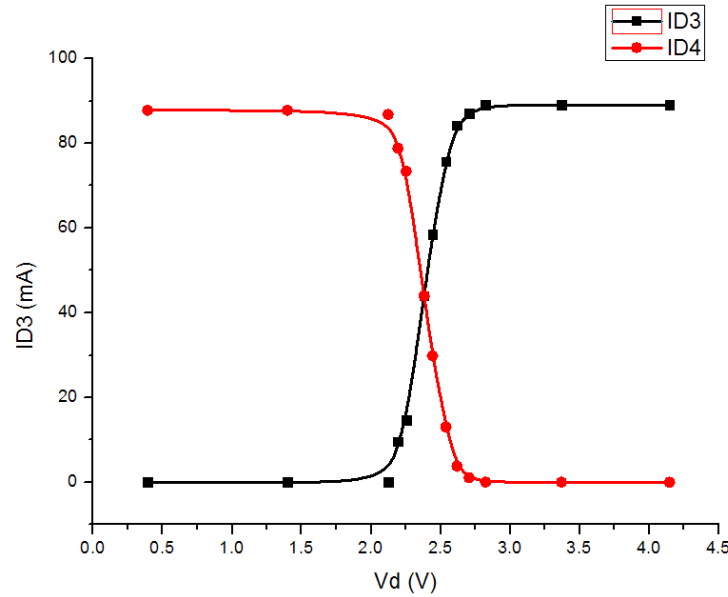


Fig. 3 The current switch inside the circuit

Fig. 3 shows the current switch inside the circuit, when the dropout voltage is larger than  $2.35V$ , the current source is mainly comes from D3, the current of which is supplied by the load current. In this case the quiescent current reduces to as low as  $1.5mA$ .

When the dropout voltage is about  $1.5V$ , the current of the current source is mainly comes from D4. The quiescent current at this time becomes larger, which turn up to nearly  $3mA$ , as shown in Fig. 4.

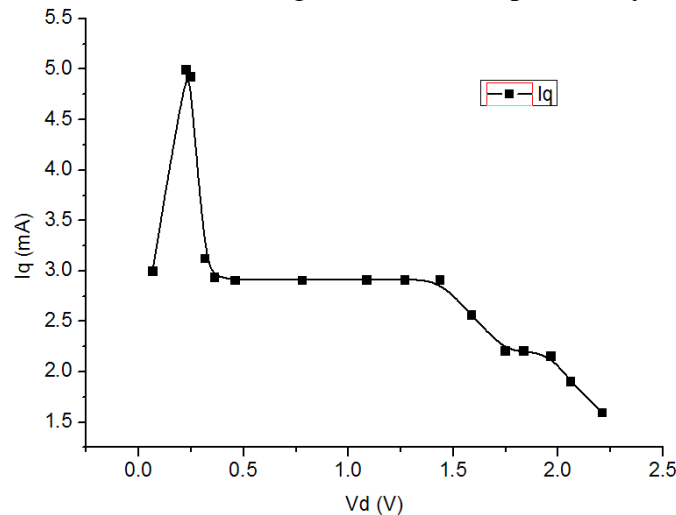


Fig. 4 The quiescent current of the circuit

### 3.3 The quiescent current limit in the circuit

When the dropout voltage fall below  $2 V_{be}$ , the transistor Q2 will be saturated ,and the output circuit will act as the emitter-follower driver.

Q5 and D2 are presented to limit the quiescent current as the input-output differential decrease to nearly zero. The base of transistor Q5 is connected to the output of error amplifier and the emitter is connected to the output by diode D2. When the output voltage is  $2 V_{be}$  lower than the base of Q5, at which time the dropout voltage is nearly zero, transistor Q5 will turn on and pull the base of transistor Q6 down which will limit any further voltage falling down of the output voltage and any further current rising of the quiescent current.

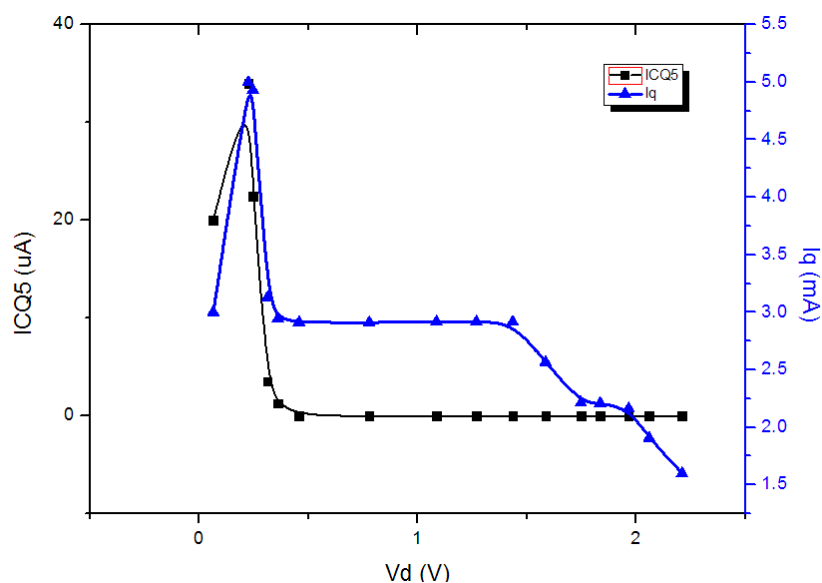


Fig. 5 The quiescent current limit in the circuit

Fig. 5 shows the transistor Q5 turn on with the collector current of 40mA, as the quiescent current increasing to 5mA, to prevent the quiescent from increasing.

#### 4. Measurement and Photograph

The LDO is implemented by a 40V high voltage bipolar technology, with a voltage supply up to -26V. The die size is 10 mm<sup>2</sup>. The chip photograph is shown in Fig. 6. The measurement in Fig7 shows that the LDO can work in a lower quiescent current at the dropout voltage above 2V.

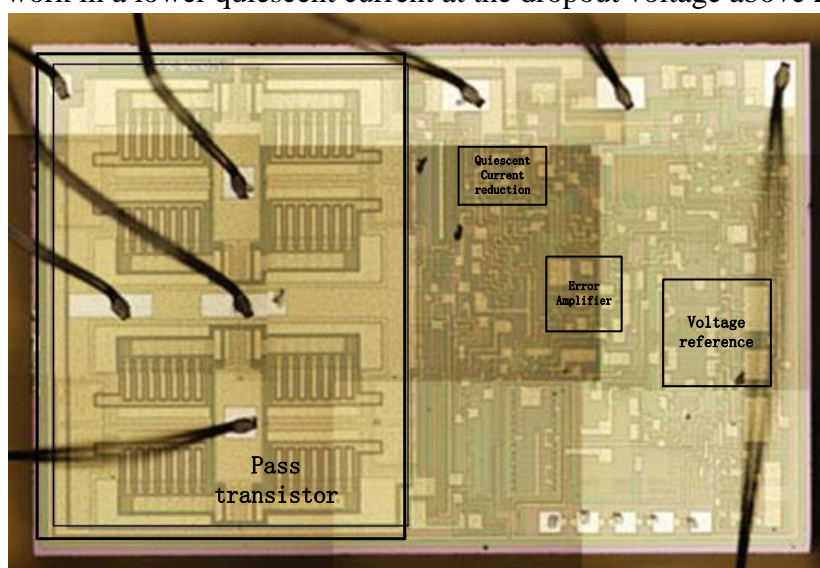


Fig. 6 Chip photograph

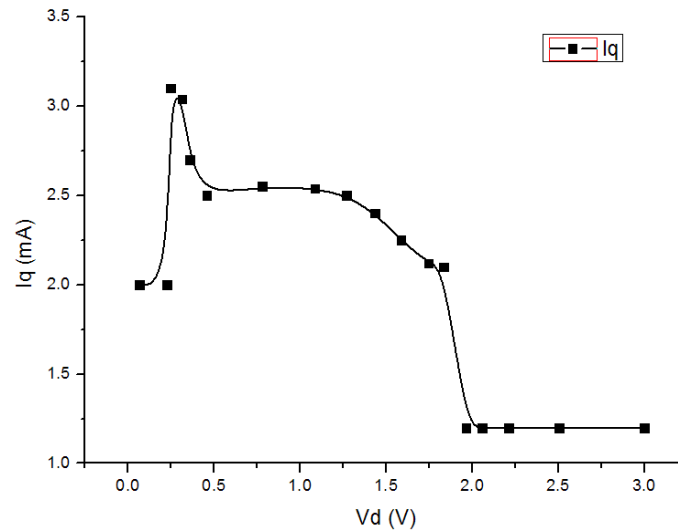


Fig. 7 Measurement result

## 5. Summary

In this paper, we have designed a negative voltage low-dropout regulator with low  $I_q$ . The structure can also be used widely in positive regulators. The measurement results show that the ground current is about 2mA and is capable to provide at least 1A load. Protection circuits including ground current limit circuit are implemented in this LDO.

## References

- [1] Shan Yuan, B.C. Kim, Low Drop-out Voltage Regulator for Wireless Applications [J], IEEE J Solid-State Circuits, June (2002), pp 23-27.
- [2] S. K. Hoon, S. Chen, F. Maloberti, A Low Noise, High Power Supply Rejection Low Dropout Regulator for Wireless System-on-chip Applications [J], IEEE J Solid-State Circuits, Sept (2005), pp 21.
- [3] Gabriel A. Rincon-Mora, Phillip E. Allen, A Low-Voltage, Low Quiescent Current Low Drop-out Regulator [J], IEEE J Solid-State Circuits, Jan (1998), pp 36-44.
- [4] Yan-xun Xu, Low Operating Current Analog Integrated Circuit [D], National Chiao-Tung University, Hsinchu, Taiwan, June 2002.
- [5] Xue-huo Yang, A Low-Quiescent Current Low-Dropout Regulator with Wide Input Range, International Journal of Electronics and Electrical Engineering, June (2015), pp 182-186.
- [6] Alan B Grebene, Bipolar And Mos Analog Integrated Circuit Design, John Wiley & Son ,Inc. (1984) 486-487.